GTK UK LTD.

Product Specifications

Customer	
Model Name	TFT029B101A
Description	320(RGB)x120 Dots 2.9" TFT LCD
Date	2017/3/17
Revision	1.0

Customer Approval	
Date	

Engineering			
Check	**Date**	**Prepared**	**Date**
Sam huang	2017/3/17	Jack guo	2017/3/17

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1 Record of Revision

Rev	Issued Date	Description	Editor
1.0	2017/3/17	First Release.	Jack Guo

2 General Specifications

Feature		Spec
Characteristics	Size	2.9inch
	Resolution	320(horizontal)*120(Vertical)
	Interface	RGB 18bit
	Connect type	Connector
	Color Depth	262k
	Technology type	a-Si
	Display Spec. Pixel pitch (mm)	0.2205 x 0.2205
	Pixel Configuration	R.G.B. Vertical Stripe
	Display Mode	Normally White
	Driver IC	SSD2116Z
	Surface Treatment	HC
	Viewing Direction	12 O'clock
Mechanical	LCM (W x H x D) (mm)	76.90*38.22*3.26
	Active Area(mm)	70.56 x 26.46
	With /Without TSP	Without TSP
	Weight (g)	TBD
	LED Numbers	6 LEDs

Note 1: RoHS
Note 2: LCM weight tolerance: +/- 5%

3 Input/Output Terminals

No.	Symbol	Description
1,2	VBL-	Backlight LED Cathode
3,4	VBL+	Backlight LED Anode.
5	Y1(YU)	Touch panel up side
6	X1(XR)	Touch panel right side
7	NC	NC
8	RESET	Reset Signal pin
9	CS	Chip select
10	SCL	Serial Clock.
11	SDA	Serial Data Input
12	SDO	Serial Data output
13	NC	NC
14~19	B0~B5	Data bus
20,21	NC	NC
22~27	G0~G5	Data bus
28,29	NC	NC
30~35	R0~R5	Data bus
36	HSYNC	Line Synchronous Signal
37	VSYNC	Frame Synchronous Signal
38	DOTCLK	Dot-clock signal and oscillator source
39	GND	Ground
40	IOVCC	Voltage input pin for logic
41	VDD	Booster input voltage pin
42	VDD	Booster input voltage pin
43	Y2(YD)	Touch panel down side
44	X2(XL)	Touch panel Left side
45-51	NC	NC
52	DEN	Display enable pin for controller
53	GND	Ground
54	GND	Ground

4 Absolute Maximum Ratings

Driving TFT LCD Panel

Item	Symbol	Conditions	Rated value	Unit	Remarks
Input voltage	VI	Ta = 25°C	-0.3 ~ V_{DDIO}+0.3	V	Note 2
Logic I/O power supply voltage	V_{DDIO}	Ta = 25°C	-0.3 ~ +4.0	V	
Analog power supply voltage	V_{CI}	Ta = 25°C	AGND-0.3 ~ +5.0	V	
Temperature for storage	Tstg	-	-30 ~ +80	°C	Note 3
Temperature for operation	Topr	-	-20 ~ +70	°C	Note 3, 4
LED input electric current	I_{LED}	Ta = 25°C	70	mA	Note 5
LED electricity consumption	P_{LED}	Ta = 25°C	238	mW	Note 5

Note 2) REST, CSB, SDI, SCK, DEN, B7~B0, G7~G0, R7~R0, VSYNC, HSYNC, DOTCLK

Note 3) Humidity: 95%RH Max. (Ta = 40°C)
Maximum bulb temperature under 39°C (Ta>40°C) See to it that no dew will be condensed.

Note 4) Panel surface temperature prescribes.

Note 5) Power consumption of one LED (Ta = 25°C) (use 6 pieces LED)

5 Electrical Characteristics

5.1 Driving TFT LCD Panel

Ta = 25°C

Item		Symbol	Min.	Typ.	Max.	Unit	Remarks
Logic I/O power supply	DC voltage	V_{DDIO}	+2.5	+3.3	+3.6	V	
	DC Current	I_{VDDIO}	-	0.35	0.50	mA	Note 6
Analog power supply	DC voltage	V_{CI}	+3.0	+3.3	+3.6	V	
	DC Current	I_{VCI}	-	13	18	mA	Note 6
Permissive input Ripple voltage		$V_{RFVDDIO}$	-	-	100	mVp-p	Note 7
		V_{RFVCI}	-	-	100	mVp-p	Note 7
Logic Input Voltage	High	V_{IH}	0.8 V_{DDIO}	-	V_{DDIO}	V	Note 8
	Low	V_{IL}	0	-	0.2 V_{DDIO}	V	Note 8
Logic Input Current	High	I_{IH}	-1	-	1	μA	Note 8
	Low	I_{IL}	-1	-	1	μA	Note 8

Note 6) $V_{DDIO} = V_{CI} = +3.3V$

Current situation for I_{VDDIO}: Black & White checker flag pattern

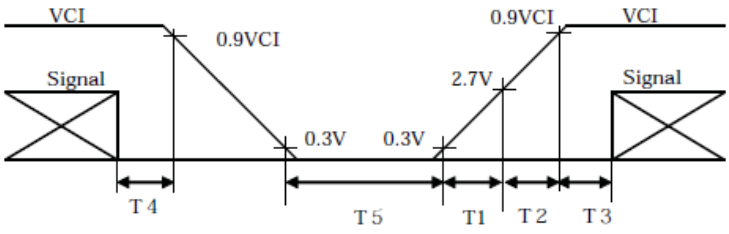
Current situation for I_{VCI}: All black patterns

Note 7) $V_{DDIO} = V_{CI} = +3.3V$

Note 8) REST, CSB, SDI, SCK, DEN, B7~B0, G7~G0, R7~R0, VSYNC, HSYNC, DOTCLK

Input voltage sequence

$0 < T1 \leqq 15$ m s
$0 < T2 \leqq 10$ m s
$0 < T3 \leqq 100$ m s
$0 < T4 \leqq 1$ s
$T5 > 200$ m s



5.2 Driving Backlight

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Forward Current	I_F	-	20	-	mA	Constant current
Forward Voltage	V_F	17.6	19.2	20.8	V	
Backlight Power consumption	W_{BL}	-	TBD	-	W	

Note 1: Each LED : IF =20 mA, VF =3.2V.
Note 2: Optical performance should be evaluated at Ta=25℃ only.
Note 3: If LED is driven by high current, high ambient temperature & humidity condition. The life time of LED will be reduced.Operating life means brightness goes down to 50% initial brightness. Typical operating life time is estimated data.

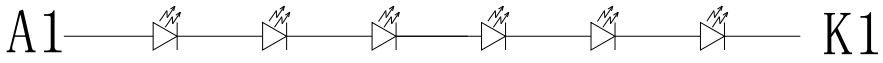
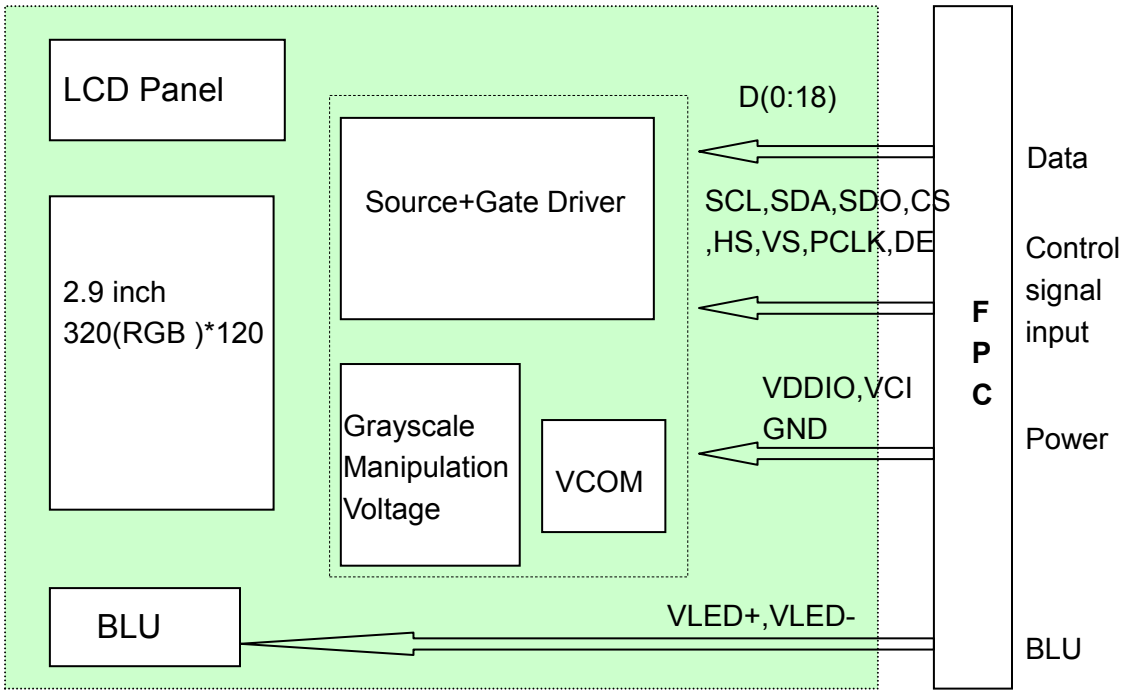


Figure : LED connection of backlight

5.3 Block Diagram



6 Interface Timing

6.1 DC Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{DDEXT}	System power supply pins of the logic block	Recommend Operating Voltage Possible Operating Voltage	1.6	-	3.6	V
V_{DDIO}	Power supply pin of IO pins	Recommend Operating Voltage Possible Operating Voltage	1.6	-	3.6	V
V_{CI}	Booster Reference Supply Voltage Range (3)	Recommend Operating Voltage Possible Operating Voltage	2.5 or V_{DDIO}	-	3.6	V
$I_{sleep}1$	Sleep mode current (VCI pin)	VDDEXT=VDDIO=1.875V, VCI=2.775V	-	30	50	uA
$I_{sleep}2$	Sleep mode current (VDDEXT+VDDIO)		-	1	50	uA
I_{dp}	Operating mode current	100pF loading at Source output VDDEXT=VDDIO=1.875V, VCI=2.775V	-	3	5	mA
V_{CIM}	Negative V_{CI} Output Voltage	No panel loading	$-V_{CI}$	-	-	V
V_{CIX2}	V_{CIX2} primary booster efficiency[1]	No panel loading, ITO for CYP, CYN, VCIX2, VCI and VCHS = 10 Ohm	90	95	-	%
			-	-	6.1	V
V_{GH}	Gate driver High Output Voltage Booster efficiency[2]	No panel loading; 4x booster; ITO for CYP, CYN, VCIX2, VCI and VCHS = 10 Ohm	84	89.5	-	%
		No panel loading; 5x booster; ITO for CYP, CYN, VCIX2, VCI and VCHS = 10 Ohm	80	88.5	-	%
		No panel loading; 6x booster; ITO for CYP, CYN, VCIX2, VCI and VCHS = 10 Ohm	72	80	-	%
V_{GL}	Gate driver Low Output Voltage		$-V_{GH}$	-	-7.3	V
V_{COMH}	VCOM High Output Voltage		VCI	-	99% x VLCD63	V
V_{COML}	VCOM Low Output Voltage		V_{CIM}+0.5	-	-	V
V_{COMA}	VCOMA		-	-	6.0 or VCIX2-0.1	V
	VCOM Amplutide V_{COMH} - V_{COML}		-	-	6.0 or VCIX2-0.1	V
V_{LCD63}	V_{LCD63} Output Voltage[3]		-	-	6.0 or VCIX2-0.1	V
ΔV_{LCD63}	Max. Source Voltage Variation		-2	-	2	%
VOH1	Logic High Output Voltage	Iout=-100 A	0.9 * V_{DDIO}	-	V_{DDIO}	V
VOL1	Logic Low Output Voltage	Iout=100 A	0	-	0.1 * V_{DDIO}	V
VIH1	Logic High Input voltage		0.8 * V_{DDIO}	-	V_{DDIO}	V
VIL1	Logic Low Input voltage		0	-	0.2 * V_{DDIO}	V
I_{OH}	Logic High Output Current Source	Vout = V_{DDIO}-0.4V	50	-	-	µA
I_{OL}	Logic Low Output Current Drain	Vout = 0.4V	-	-	-50	µA
I_{OZ}	Logic Output Tri-state Current Drain Source		-1	-	1	µA
I_{IL}/I_{IH}	Logic Input Current		-1	-	1	µA
C_{IN}	Logic Pins Input Capacitance		-	5	7.5	pF
R_{SON}	Source drivers output resistance		-	1	-	kΩ
R_{GON}	Gate drivers output resistance		-	500	-	Ω
R_{COM}	VCOM output resistance		-	200	-	Ω
TC	Temperature Coefficient		-	-0.01	-	%

Note1: V_{CIX2} **efficiency** = V_{CIX2} /(2 x V_{CI}) x 100%
Note2: V_{GH} **efficiency** = V_{GH}/(V_{CI} x n) x 100% **(where n = booster factor)**
Note3: **VCIX2 – VLCD63 ≥ 0.1V**

6.2 AC Characteristics

AC Characteristics (Unless otherwise specified, Voltage Referenced to V_{SS}, V_{DDIO} = 1.875V, T_A = -40 to 85°C)

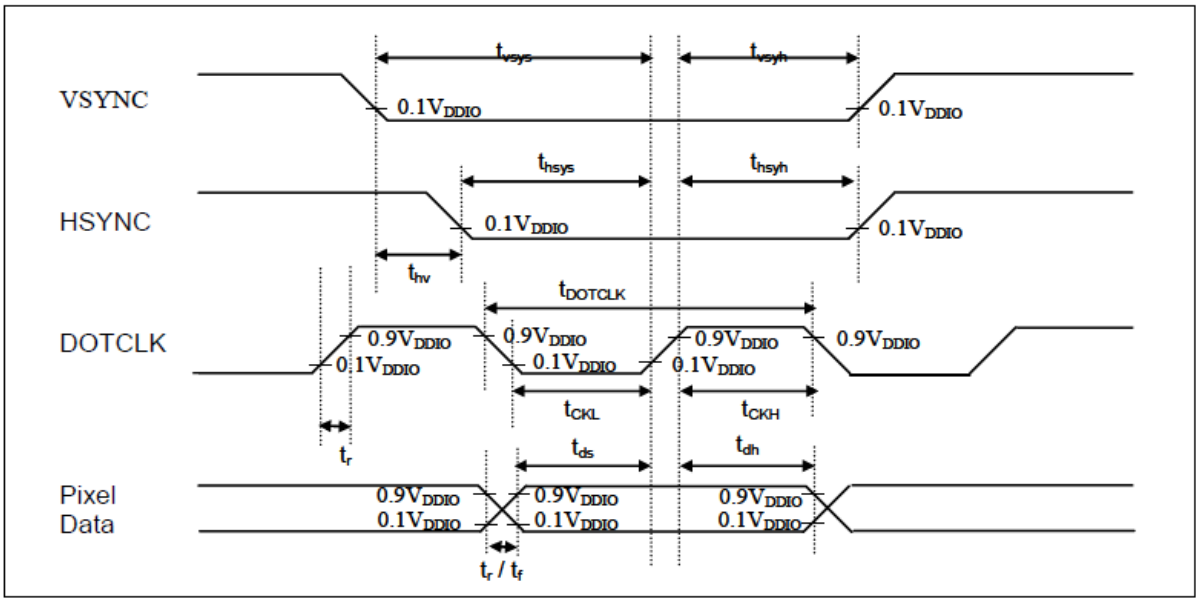
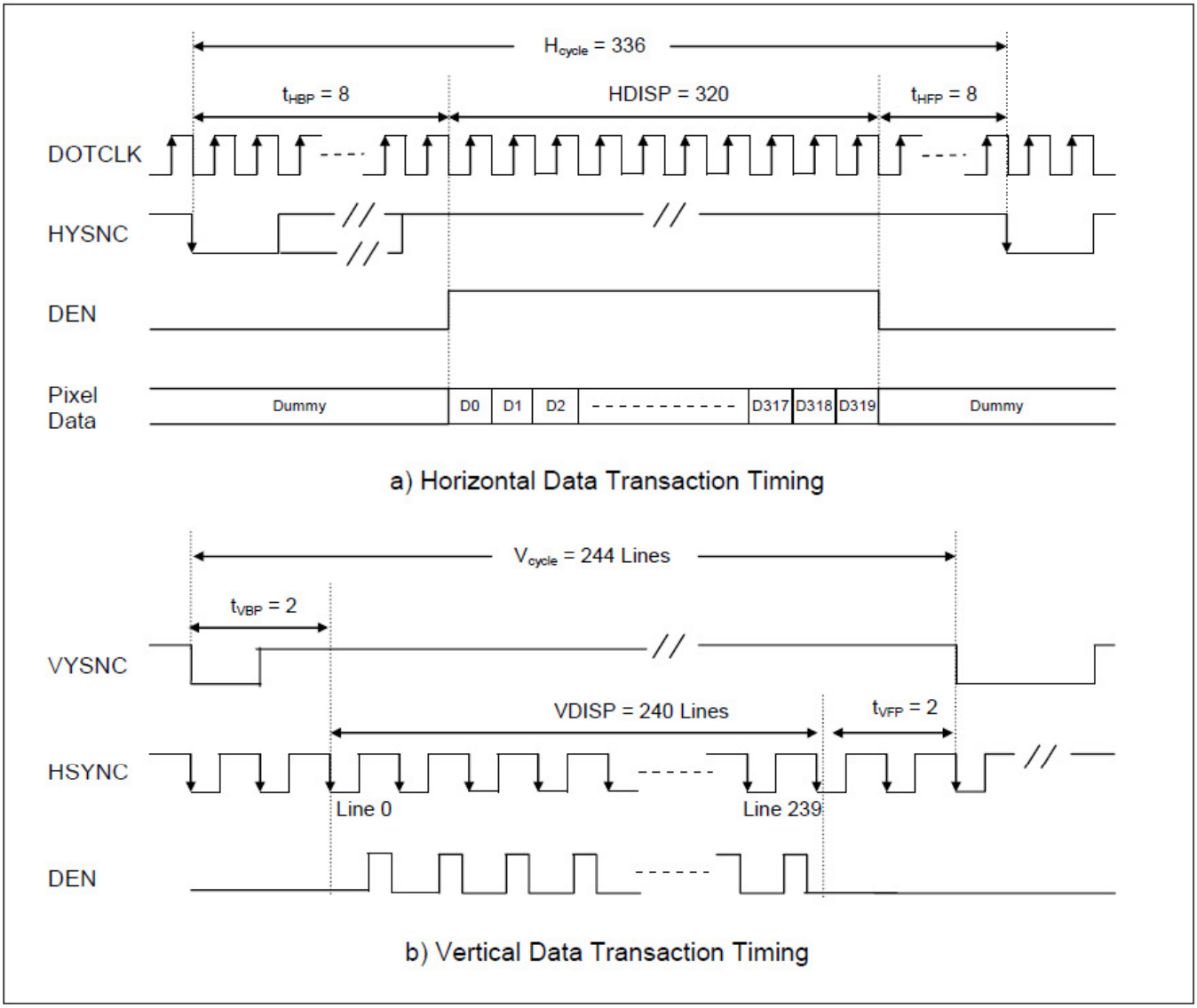


Figure 15-1- Pixel Clock Timing

Characteristics	Symbol	Min	Typ	Max	Units
DOTCLK Frequency	f_{DOTCLK}	-	5.0	8.6	MHz
DOTCLK Period	t_{DOTCLK}	116	200	-	nSec
Vertical Sync Setup Time	t_{vsys}	20	-	-	nSec
Vertical Sync Hold Time	t_{vsyh}	20	-	-	nSec
Horizontal Sync Setup Time	t_{hsys}	20	-	-	nSec
Horizontal Sync Hold Time	t_{hsyh}	20	-	-	nSec
Phase difference of Sync Signal Falling Edge	t_{hv}	0	-	320	t_{DOTCLK}
DOTCLK Low Period	t_{CKL}	58	-	-	nSec
DOTCLK High Period	t_{CKH}	58	-	-	nSec
Data Setup Time	t_{ds}	30	-	-	nSec
Data hold Time	t_{dh}	30	-	-	nSec
Reset pulse width	t_{RES}	10	-	-	uSec
Rise / Fall time	t_r / t_f	-	-	100	nSec

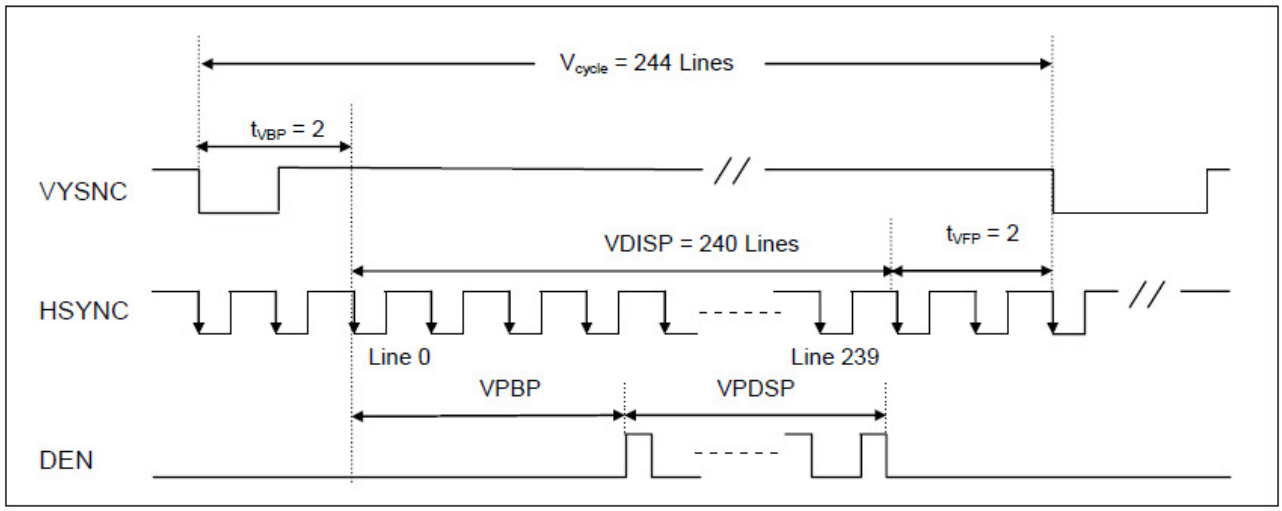
Note: External clock source must be provided to DOTCLK pin of SSD2116Z. The driver will not operate if absent of the clocking signal.

Figure 15-2 Data Transaction Timing in Normal Operating Mode (262k-color)



Characteristics	Symbol	Min	Typ	Max	Unit
DOTCLK Frequency	f_{DOTCLK}	-	5.0	8.6	MHz
DOTCLK Period	t_{DOTCLK}	116	200	-	nSec
Horizontal Frequency (Line)	f_H	-	14.9	-	kHz
Vertical Frequency (Refresh)	f_V	-	60.9	-	Hz
Horizontal Back Porch	t_{HBP}	-	8	-	t_{DOTCLK}
Horizontal Front Porch	t_{HFP}	-	8	-	t_{DOTCLK}
Horizontal Data Start Point	t_{HBP}	-	8	-	t_{DOTCLK}
Horizontal Blanking Period	$t_{HBP} + t_{HFP}$	-	16	-	t_{DOTCLK}
Horizontal Display Area	HDISP	-	320	-	t_{DOTCLK}
Horizontal Cycle	H_{cycle}	-	336	511	t_{DOTCLK}
Vertical Back Porch	t_{VBP}	-	2	126	Line
Vertical Front Porch	t_{VFP}	-	2	126	Line
Vertical Data Start Point	t_{VBP}	-	2	126	Line
Vertical Blanking Period	$t_{VBP} + t_{VFP}$	-	4	252	Line
Vertical Display Area	VDISP	-	240	-	Line
Vertical Cycle	V_{cycle}	-	244	-	Line

Figure 15-3- Synchronization Signals Timing in Power Save Mode (8 color)



Characteristics	Symbol	Min	Typ	Max	Units
DOTCLK Frequency	f_{DOTCLK}	-	5.0	8.6	MHz
DOTCLK Period	t_{DOTCLK}	116	200	-	nSec
Horizontal Frequency (Line)	f_H	-	14.9	-	kHz
Vertical Frequency (Refresh)	f_V	-	60.9	-	Hz
Vertical Partial Back Porch	VPBP	0	-	239	Line
Vertical Active Area	VPDSP	1	-	240	Line
Vertical Back Porch	t_{VBP}	-	2	126	Line
Vertical Front Porch	t_{VFP}	-	2	126	Line
Vertical Display Area	VDISP	-	240	-	Line
Vertical Cycle	V_{cycle}	-	244	-	Line

Note: When entered to 8-color display mode, the RGB graphic data through the interface pins RR5, GG5 and BB5 are valid within the Vertical Active Area. Data "0" will be displayed outside the Vertical Active Area.

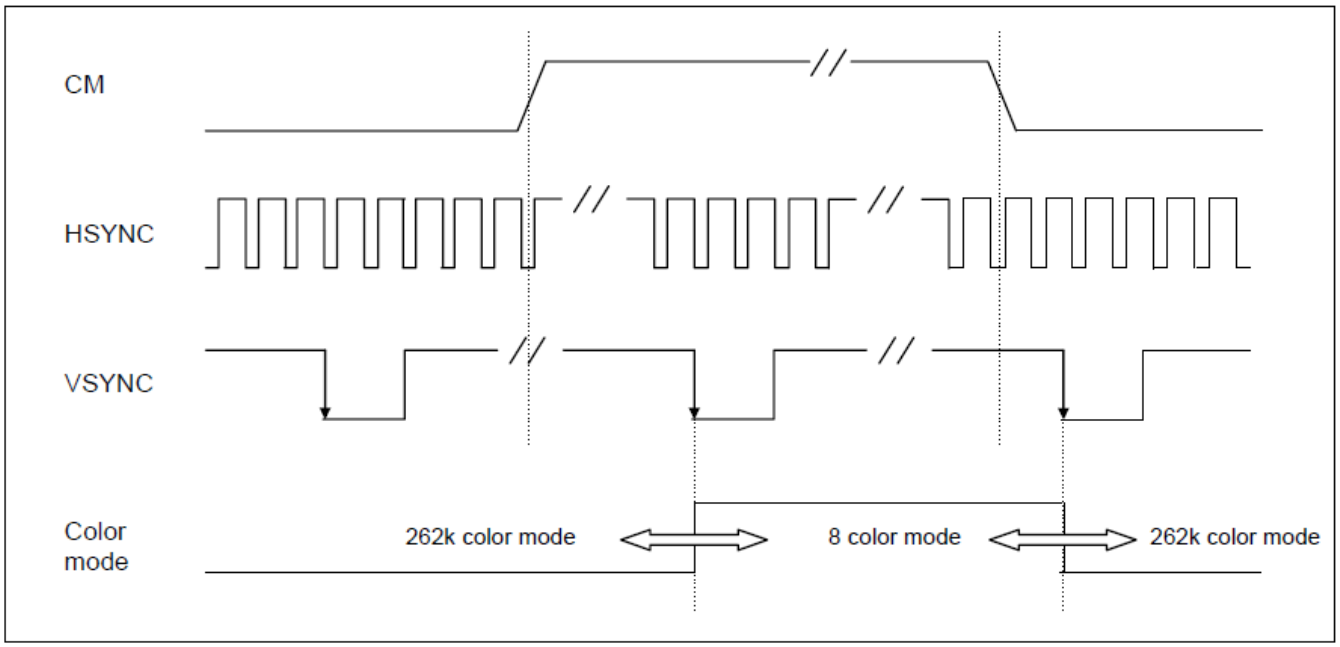


Figure 15-4- Color Mode Conversion Timing

Note: The color mode conversion starts at the first falling edge of VSYNC after stage change of CM.

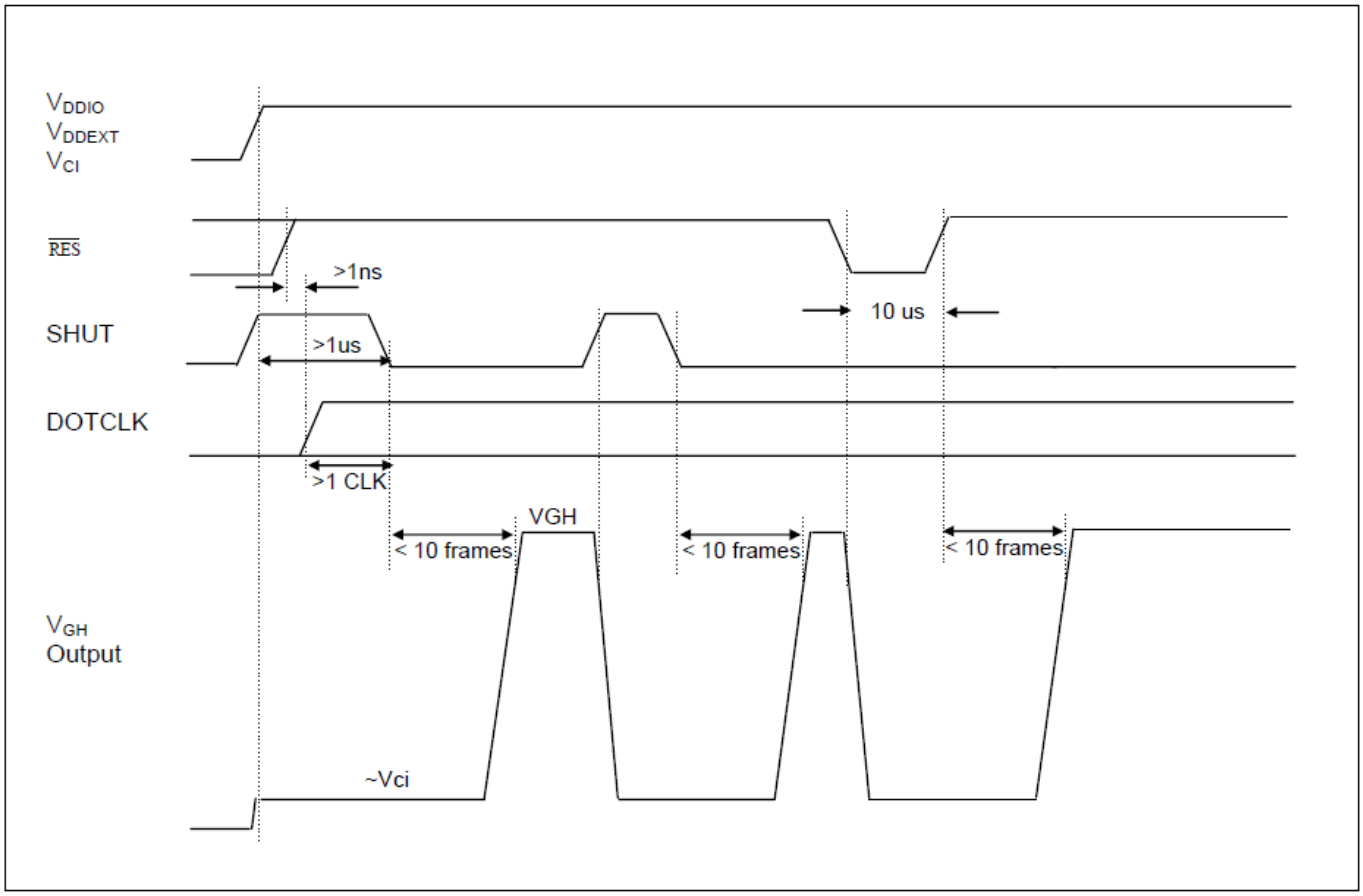


Figure 15-5- VGH Output against SHUT & RESB

Note1: **The minimum cycle time of SHUT is 10 + 2 frames.**

Note2: **DOTCLK must be provided for boosting of V_{GH}. The above timing diagram assumed voltages and DOTCLK are continuous supplied after power on.**

Note3: **V_{GH} will be forced to V_{Ci} at the low stage of $\overline{RES}$.**

Note4: **The minimum pulse width of RESET is 10us.**

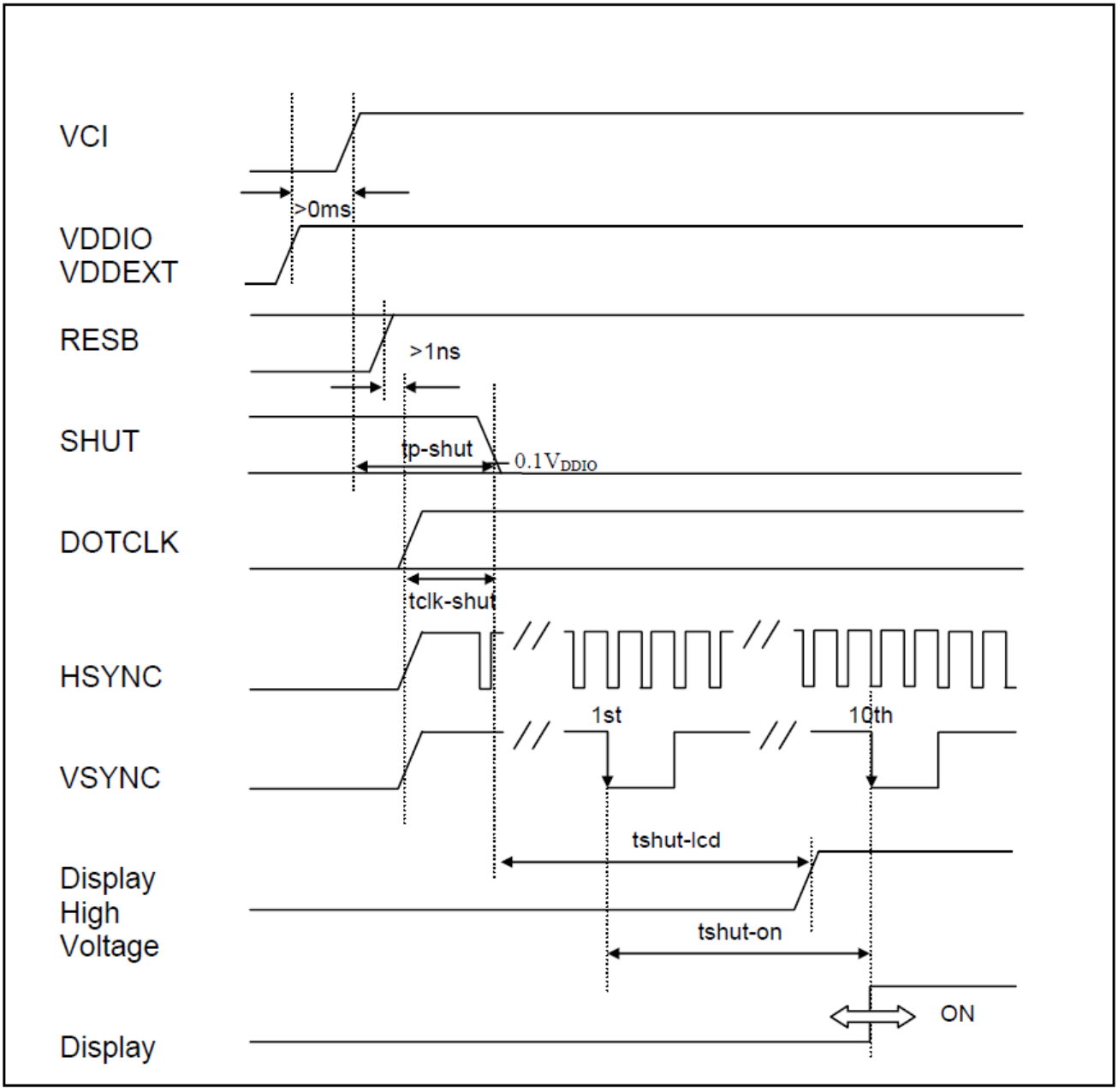


Figure 15-6 - Power Up Sequence

Characteristics	Symbol	Min	Typ	Max	Units
V_{DDEXT} / V_{DDIO} on to falling edge of SHUT	tp-shut	1	-	-	µsec
DOTCLK	tclk-shut	1	-	-	clk
Falling edge of SHUT to LCD power on	tshut-lcd	-	-	164	msec
Falling edge of SHUT to display start	tshut-on	-	-	10	frame
-- 1 line: 336 clk -- 1 frame: 244 line -- DOTCLK = 5.0MHz		-	164	-	msec

Note1: **It is necessary to input DOTCLK before the falling edge of SHUT.**

Note2: **Display starts at 10th falling edge of VSTNC after the falling edge of SHUT.**

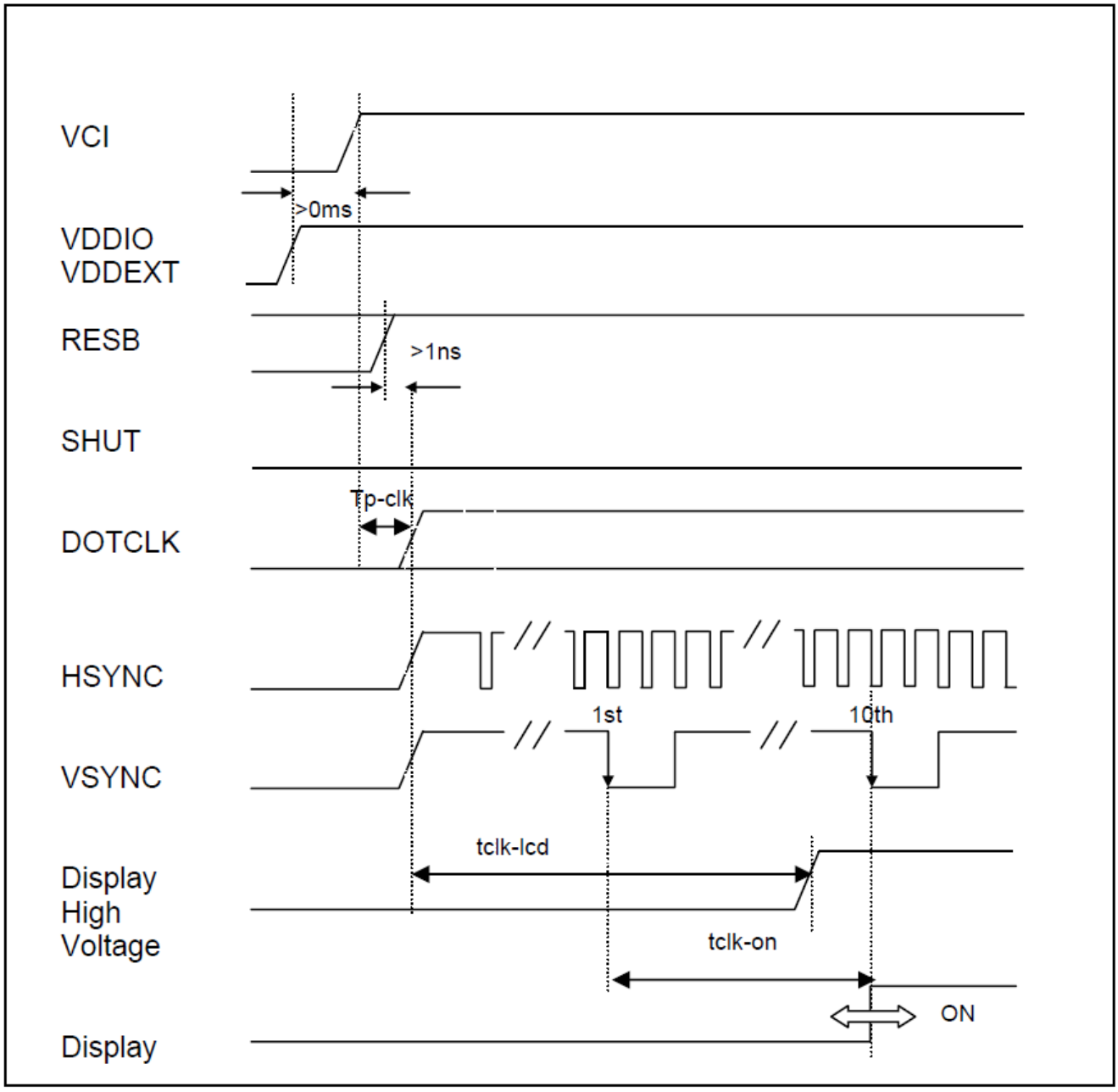


Figure 15-7 - Power Up Sequence (Shut pin tied to ground)

Characteristics	Symbol	Min	Typ	Max	Units
V_{DDEXT} / V_{DDIO} on to rising edge of Dotclk	tp-clk	1	-	-	µsec
Rising edge of Dotclk to LCD power on	tclk-lcd	-	-	164	msec
Rising edge of Dotclk to display start	tclk-on	-	-	10	frame
-- 1 line: 336 clk -- 1 frame: 244 line -- DOTCLK = 5.0MHz		-	164	-	msec

Note1: Display starts at 10th falling edge of VSYNC after the rising edge of DOTCLK.

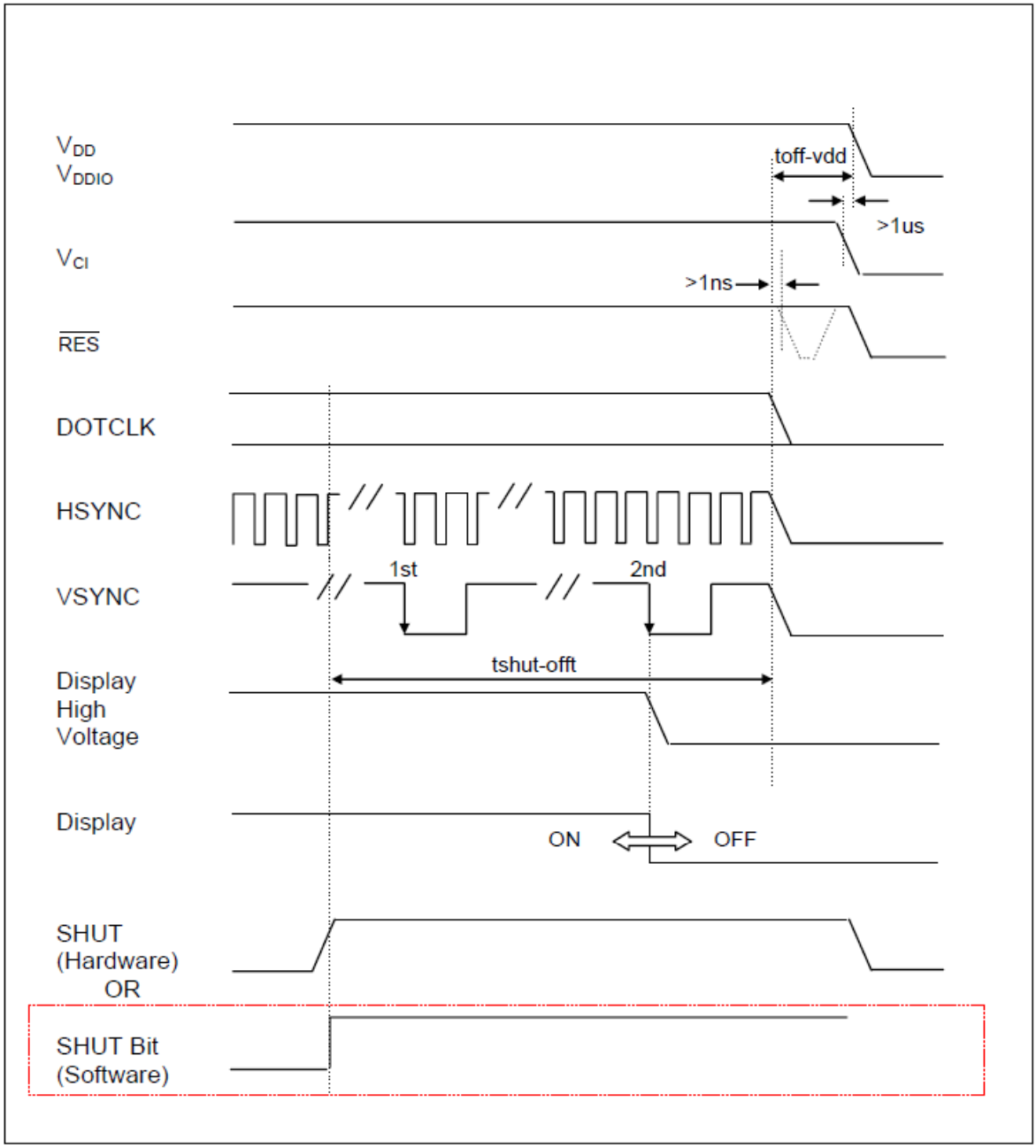


Figure 15-8 - Power Down Sequence

Characteristics	Symbol	Target Min	Target Typ	Target Max	Units
Rising edge of SHUT to display off -- 1 line: 336 clk -- 1 frame: 244 line -- PIXCLK = 5.0 MHz	tshut-off	2	-	-	frame
		32.8	-	-	msec
Input-signal-off to V_{DDEXT} / V_{DDIO} off	toff-vdd	1	-	-	µsec

Note1: DOTCLK must be maintained at lease 2 frames after the rising edge of SHUT.

Note2: Display become off at the 2nd falling edge of VSTNC after the falling edge of SHUT.

Note3: If RESET signal is necessary for power down, provide it after the 2-frames-cycle of the SHUT period.

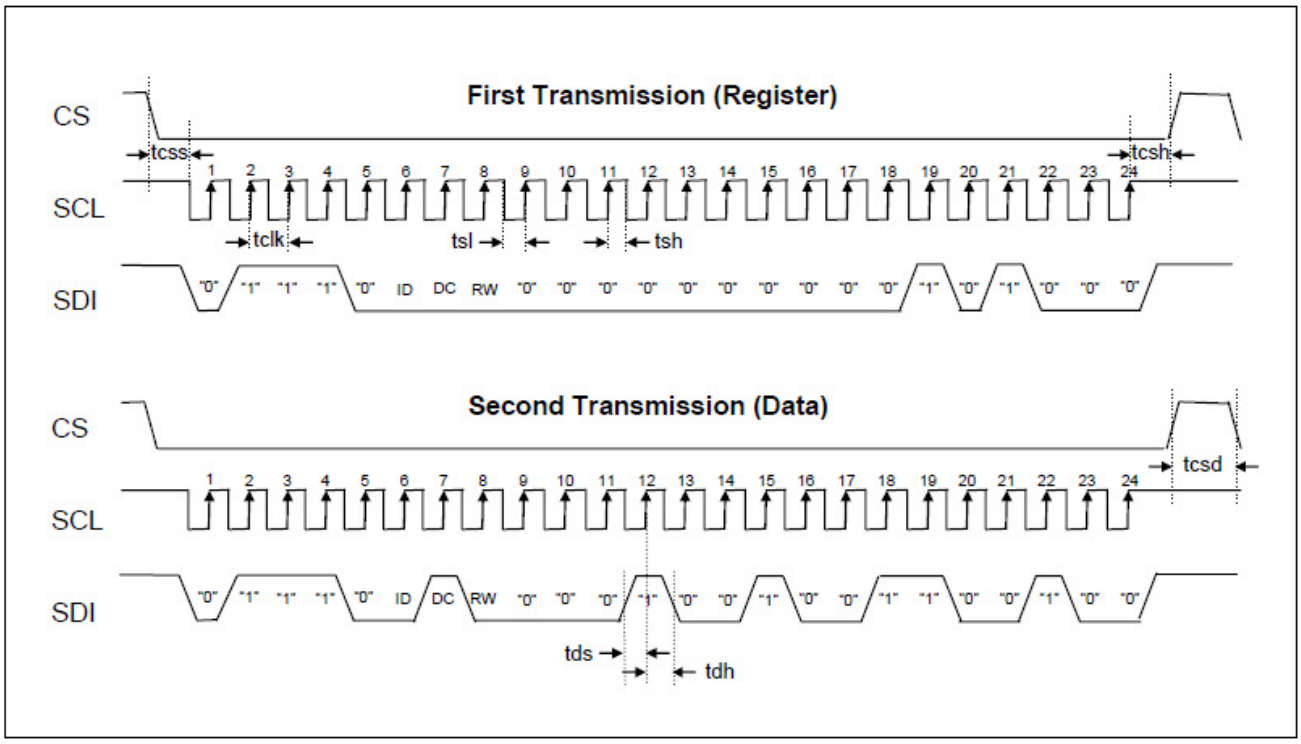


Figure 15-9 - SPI Interface Timing Diagram & Transaction Example

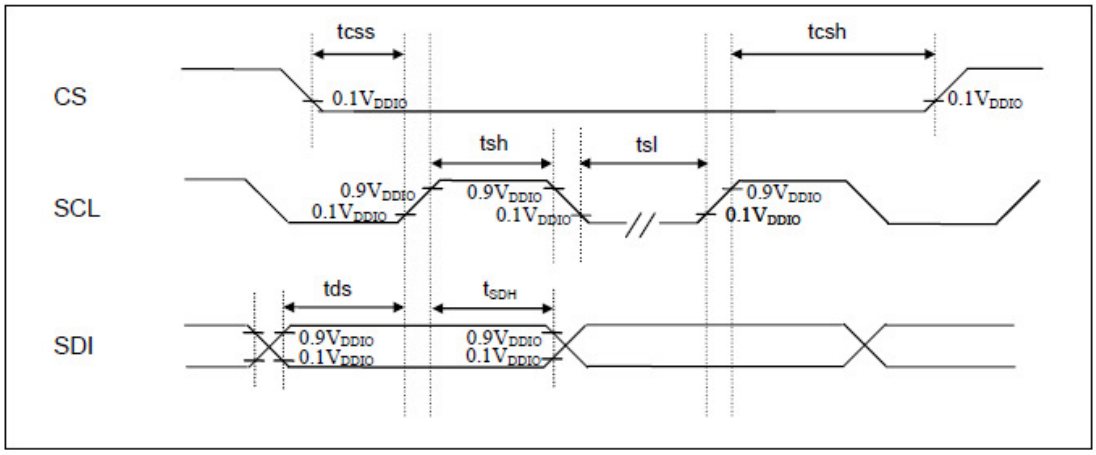


Figure 15-10 - SPI Interface Timing Diagram

Characteristics	Symbol	Min	Typ	Max	Units
Serial Clock Frequency	fclk	-	-	20	MHz
Serial Clock Cycle Time	tclk	50	-	-	nsec
Clock Low Width	tsl	25	-	-	nsec
Clock High Width	tsh	25	-	-	nsec
Chip Select Setup Time	tcss	0	-	-	nsec
Chip Select Hold Time	tcsh	10	-	-	nsec
Chip Select High Delay Time	tcsd	20	-	-	nsec
Data Setup Time	tds	5	-	-	nsec
Data Hold Time	tdh	10	-	-	nsec

Note1: The example transmit "0x1264h" to register R28h.

Note2: SPID pin connected to VSS.

7 Optical Characteristics

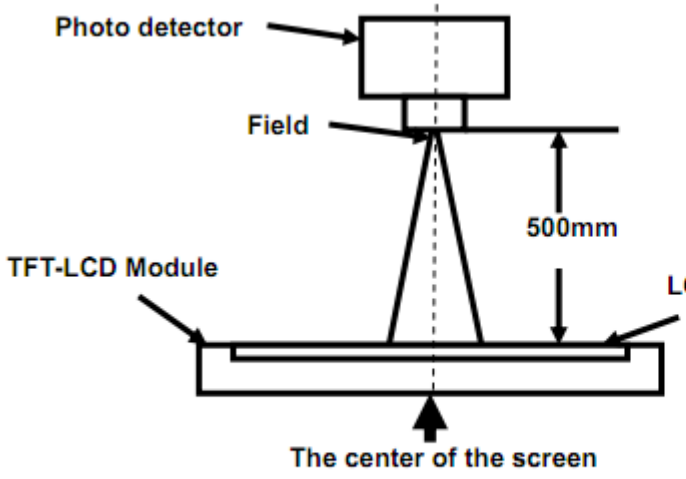
Items		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing angles		θ_T	Center CR≥10	-	40	-	Degree.	Note2
		θ_B		-	60	-		
		θ_L		-	60	-		
		θ_R		-	60	-		
Contrast Ratio		CR	Θ =0	100	300	-	-	Note1, Note3
Response Time		T_{ON}	25° C	-	30	45	ms	Note1, Note4
		T_{OFF}		-	30	45		
Chromaticity	White	X_W	Backlight is on	0.25	0.30	0.35	-	Note1, Note5
		Y_W		0.27	0.32	0.37	-	
	Red	X_R		0.52	0.57	0.62	-	
		Y_R		0.26	0.31	0.36	-	
	Green	X_G		0.29	0.34	0.39	-	
		Y_G		0.50	0.55	0.60	-	
	Blue	X_B		0.10	0.15	0.20	-	
		Y_B		0.05	0.10	0.15	-	
Uniformity		U		75	80	-	%	Note1, Note6
NTSC					50		%	Note5
Luminance		L		-	300	-		Note1, Note7

Test Conditions:

1. IF= 20mA(one channel),the ambient temperature is 25
2. The test systems refer to Note 1 and Note 2.

Note 1:Definition of optical measurement system.

The optical characteristics should be measured in dark room. After 5 minutes operation, the optical properties are measured at the center point of the LCD screen. All input terminals LCD panel must be ground when measuring the center area of the panel.



Item	Photo detector	Field
Contrast Ratio	SR-3A	1°
Luminance		
Chromaticity		
Lum Uniformity		
Response Time	BM-7A	2°

Note 2: Definition of viewing angle range and measurement system.
viewing angle is measured at the center point of the LCD by CONOSCOPE(ergo-80).

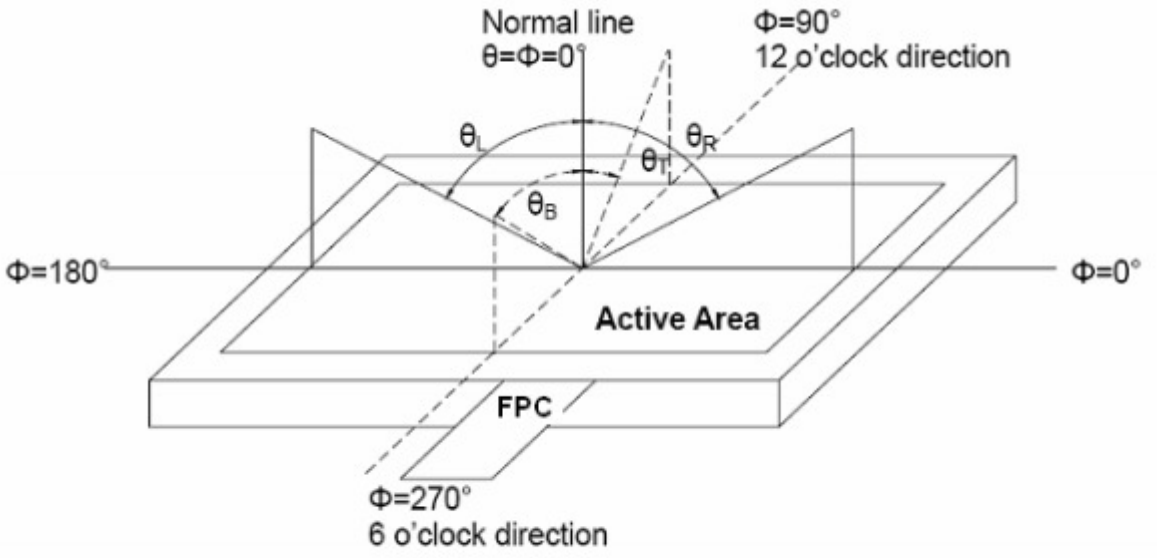


Fig. 1 Definition of viewing angle

Note 3: Definition of contrast ratio

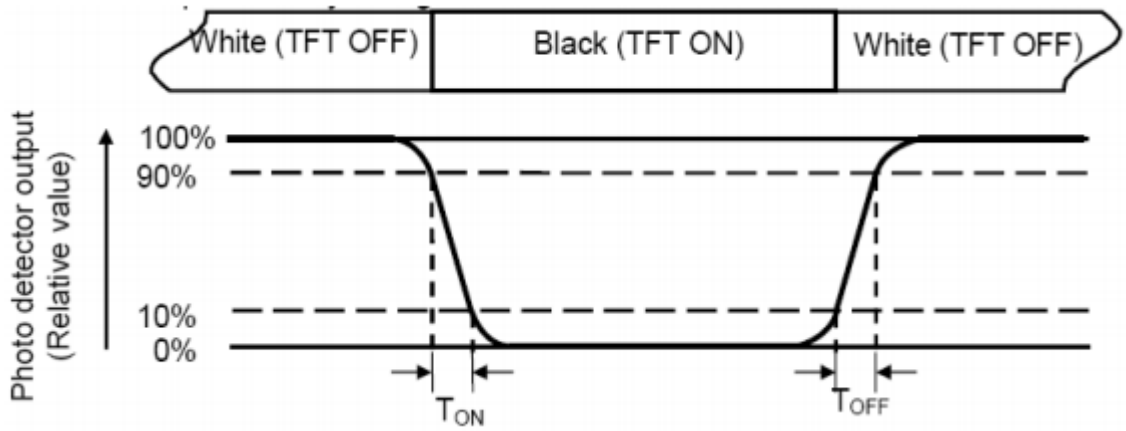
$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD is on the "White" state}}{\text{Luminance measured when LCD is on the "Black" state}}$$

“White state “:The state is that the LCD should driven by Vwhite.

“Black state”: The state is that the LCD should driven by Vblack.

Vwhite: To be determined Vblack: To be determined.

Note 4: Definition of Response time
The response time is defined as the LCD optical switching time interval between “White” state and “Black” state. Rise time (TON) is the time between photo detector output intensity changed from 90% to 10%. And fall time (TOFF) is the time between photo detector output intensity changed from 10% to 90%.



Note 5: Definition of color chromaticity (CIE1931)
Color coordinates measured at center point of LCD.

Note 6: Definition of Luminance Uniformity
Active area is divided into 9 measuring areas (Refer Fig. 2). Every measuring point is placed at the center of each measuring area.

Luminance Uniformity(U) = Lmin/ Lmax

L-------Active area length W----- Active area width

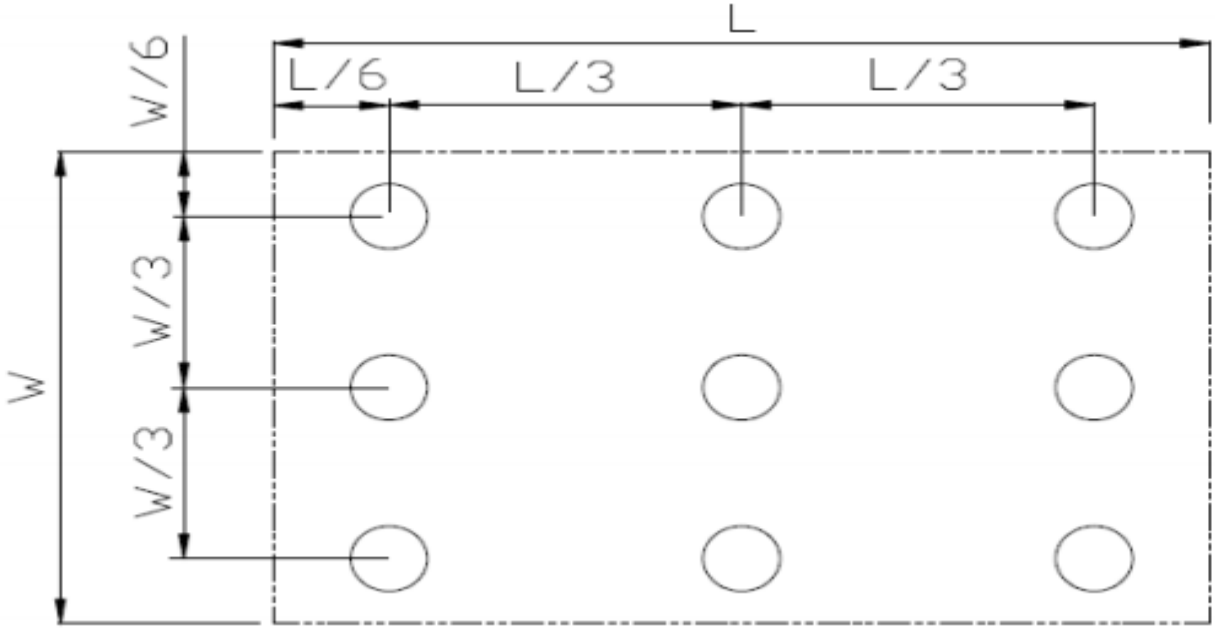


Fig. 2 Definition of uniformity
Lmax: The measured maximum luminance of all measurement position.
Lmin: The measured minimum luminance of all measurement position.

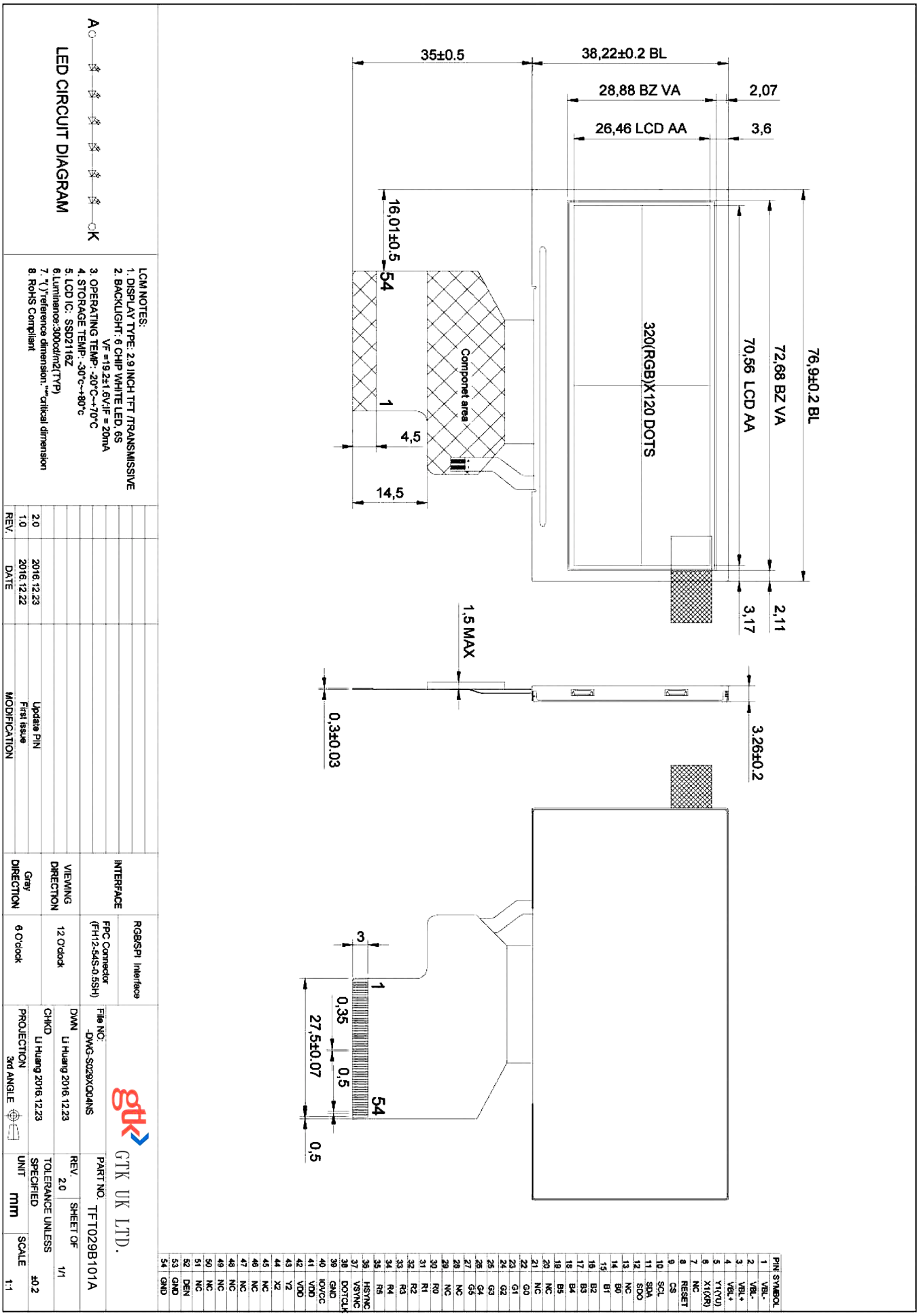
Note 7: Definition of Luminance :
Measure the luminance of state at point.

8 Environmental / Reliability Tests

No	Test Item	Condition	Remarks
1	High Temperature Operation	Ts= +70℃, 120hrs	Note 1 IEC60068-2-2, GB2423. 2-89
2	Low Temperature Operation	Ta= -20℃, 120hrs	Note 2 IEC60068-2-1 GB2423.1-89
3	High Temperature Storage	Ta= +80℃, 240hrs	IEC60068-2-2 GB2423. 2-89
4	Low Temperature Storage	Ta= -30℃, 240hrs	IEC60068-2-1 GB/T2423.1-89
5	High Temperature & Humidity Storage	Ta= +60℃, 90% RH max, 160 hours	IEC60068-2-3 GB/T2423.3-2006
6	Thermal Shock (Non-operation)	-30℃ 30 min ~ +80℃ 30 min Change time: 5min, 30 Cycle	Start with cold temperature,end with high temperature IEC60068-2-14, GB2423.22-87
7	Electro Static Discharge (Opeartion)	C=150pF, R=330 Ω, 5 points/panel Air:±8KV, 5 times; Contact: ±4KV, 5 times; (Environment: 15℃ ~ 35℃, 30% ~ 60%, 86Kpa ~ 106Kpa)	IEC61000-4-2 GB/T17626.2-1998
8	Vibration (Non-operation)	Frequency range: 10~55Hz, Stroke: 1.mm Sweep: 10Hz~55Hz~10Hz 2 hours for each direction of X .Y. Z. (package condition)	IEC60068-2-6 GB/T2423.5-1995
9	Shock (Non-operation)	60G 6ms, ± X, ±Y, ± Z 3 times for each direction	IEC60068-2-27 GB/T2423.5-1995
10	Package Drop Test	Height: 80 cm, 1 corner, 3 edges, 6 surfaces	IEC60068-2-32 GB/T2423.8-1995

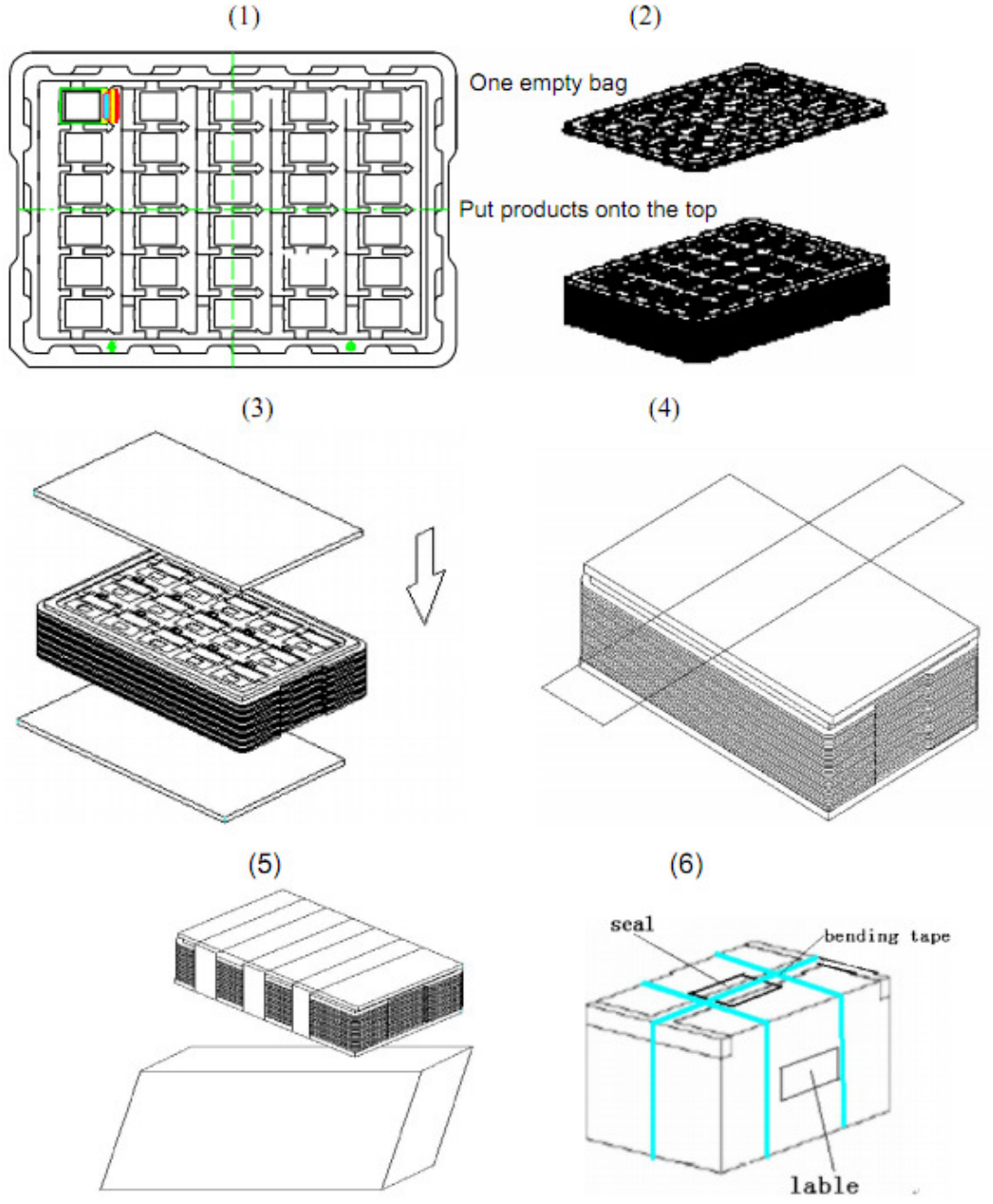
Note: 1. T_S is the temperature of panel's surface.
2. Ta is the ambient temperature of sample.

9 Mechanical Drawing



1 0.Packing

Packing Method



1. Put module into tray cavity:
2. Tray stacking
3. Put 1 cardboard under the tray stack and 1 cardboard above:
4. Fix the cardboard to the tray stack with adhesive tape:
5. Put the tray stack into carton.
6. Carton sealing with adhesive tape.

11 Precautions For Use of LCD modules

11.1 Handling Precautions

11.1.1. The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

11.1.2. If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.

11.1.3. Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

11.1.4. The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.

11.1.5. If the display surface is contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:

- Isopropyl alcohol
- Ethyl alcohol

Solvents other than those mentioned above may damage the polarizer. Especially, do not use the following:

- Water
- Ketone
- Aromatic solvents

11.1.6. Do not attempt to disassemble the LCD Module.

11.1.7. If the logic circuit power is off, do not apply the input signals.

11.1.8. To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

11.1.8.1. Be sure to ground the body when handling the LCD Modules.

11.1.8.2. Tools required for assembly, such as soldering irons, must be properly ground.

11.1.8.3. To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.

11.1.8.4. The LCD Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

11.2 Storage Precautions

12.2.1. When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps.

11.2.2. The LCD modules should be stored under the storage temperature range If the LCD modules will be stored for a long time, the recommend condition is:

Temperature : 0℃ ～ 40℃ Relatively humidity: ≤80%

11.2.3. The LCD modules should be stored in the room without acid, alkali and harmful gas.

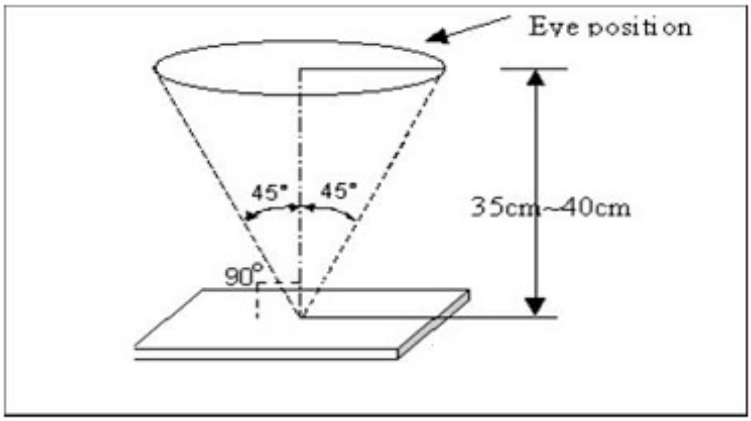
11.3 Inspection Sampling

3.1. Lot size : Quantity per shipment lot per model

3.2. Sampling type: Normal inspection, Single sampling
3.3. Inspection level: II
3.4. Sampling table : MIL-STD-105D
3.5. Acceptable quality level （AQL ）
Major defect : AQL=0.65
Minor defect: AQL=1.00

11.4 Inspection Conditions

4.1 Ambient conditions:
a. Temperature: Room temperature 25±5℃
b. Humidity: (60±10) ％RH
c. Illumination: Single fluorescent lamp non-directive (300 to 700 Lux)
4.2 Viewing distance
The distance between the LCD and the inspector’ s eyes shall be at least 35±5 ㎝.
4.3 Viewing Angle
U/D: 45o/45o, L/R: 45o/45o



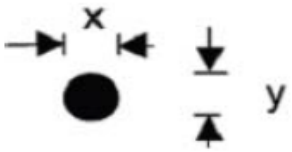
11.5. Inspection Criteria

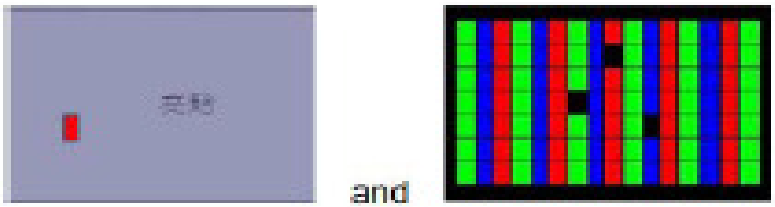
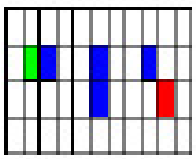
Defects are classified as major defects and minor defects according to the degree of defectiveness defined herein.

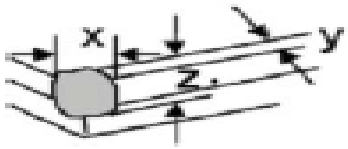
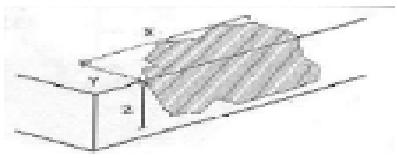
11.5.1 Major defect

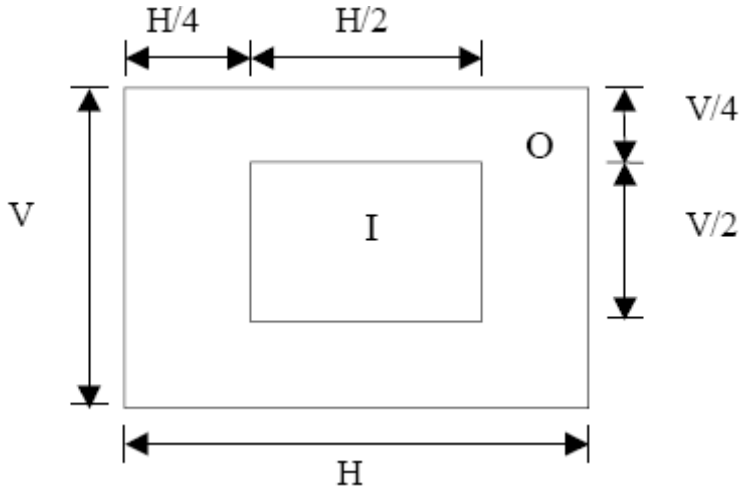
Item No	Items to be inspected	Inspection Standard
5.1.1	All functional defects	1) No display 2) Display abnormally 3) Short circuit 4) line defect
`5.1.2	Missing	Missing function component
5.1.3	Crack	Glass Crack

11.5.2 Minor defect

<table>
<tr><th>Item No</th><th>Items to be inspected</th><th colspan="2">Inspection standard</th></tr>
<tr><td rowspan="5">5.2.1</td><td rowspan="5">Spot Defect
Including
Black spot
White spot
Pinhole
Foreign particle</td><td colspan="2">For dark/white spot is defined
φ = (x+y) /2
 
</td></tr>
<tr><td>Size φ(mm)</td><td>Acceptable Quantity</td></tr>
<tr><td>φ≤0.10</td><td>Ignore</td></tr>
<tr><td>0.10 < ϕ≤0.2</td><td>2</td></tr>
<tr><td>0.2 < ϕ</td><td>Not allowed</td></tr>
</table>

<table>
<tr><td rowspan="2">5.2.2</td><td rowspan="2">Polarizer dirt, particle</td><td>Size φ(mm)</td><td>Acceptable Quantity</td></tr>
<tr><td>φ≤0.15</td><td>1</td></tr>
<tr><td rowspan="5">5.2.3</td><td rowspan="5">Line Defect
Including Black line White line Scratch</td><td colspan="2">Define:
 
</td></tr>
<tr><td>Width(mm)
Length(mm)</td><td>Acceptable Quantity</td></tr>
<tr><td>W≤0.05</td><td>Ignore</td></tr>
<tr><td>0.05 < W≤0.1
L≤1.5</td><td>2</td></tr>
<tr><td>0.1 < W, or L>1.5</td><td>Not allowed</td></tr>
<tr><td>5.2.4</td><td>Polarizer Dent/Bubble</td><td colspan="2">Not allowed</td></tr>
<tr><td rowspan="8">5.2.5</td><td rowspan="8">Electrical Dot Defect</td><td colspan="2">Bright and Black dot define:
 
and
 
Two Adjacent Dot</td></tr>
<tr><td colspan="2">Inspection patteru: Full white. Full black. Red. green and blue screens</td></tr>
<tr><td rowspan="2">Item</td><td colspan="3">Acceptable Quantity</td></tr>
<tr><td>I</td><td>O</td><td>Note</td></tr>
<tr><td>Black dot defect</td><td colspan="2">2</td><td rowspan="2">5mm≤Distance</td></tr>
<tr><td>Bright dot defect</td><td colspan="2">1</td></tr>
<tr><td>Two Adjacent Dot</td><td colspan="2">1</td><td></td></tr>
<tr><td>There or more Adjacent Dot</td><td colspan="3">Not allowed</td></tr>
<tr><td>Total Dot</td><td colspan="2">2</td><td></td></tr>
</table>

<table>
<tr><td rowspan="4">5.2.6</td><td rowspan="4">Glass defect</td><td colspan="2">1.Corner Fragment:
  </td></tr>
<tr><td>Size(mm)</td><td>Acceptable Quantity</td></tr>
<tr><td>X≤2mm
Y≤1mm
Z≤T</td><td>Ignore
T：Glass thickness
X: Length
Y: Width
Z: thickness</td></tr>
<tr><td colspan="2">2. Side Fragment:
  </td></tr>
<tr><td>Size(mm)</td><td>Acceptable Quantity</td></tr>
<tr><td>X≤5.0mm
Y ≤1mm
Z≤T</td><td>T：Glass thickness
X: Length
Y: Width
Z: thickness</td></tr>
</table>



Note: 1). Dot defect is defined as the defective area of the dot area is larger than 50% of the dot area.

2). The distance between two bright dot defects (red, green, blue, and white) should be larger than 15mm.

3). The distance between black dot defects or black and bright dot defects should be more than 5mm apart.

4). Polarizer bubble is defined as the bubble appears on active display area. The defect of polarizer bubble shall be ignored if the polarizer bubble appears on the outside of active display area.

11.6 Mechanics specification

As for the outside dimension of the modules, please refer to product specification for more details

Note: 1). Dot defect is defined as the defective area of the dot area is larger than 50% of the dot area.
2). The distance between two bright dot defects (red, green, blue, and white)