SPECIFICATION
FOR
TFT MODULE

MODULE NO. :IPS078A110A

CUSTOMER NO. :

Rev No. : O

GTK	PREPARED BY	CHECKED BY	APPROVED BY
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DATE	2020.12.07	2020.12.07	2020.12.07

	SIGNATURE	DATE
CUSTOMER APPROVAL		

Notes :

1、Please contact GTK before assigning your product based on this module specification.

2、To improve the quality of product, and this product specification is subject to change without any notice.

REVISION RECORD

Rev No.	Rev date	Contents	Remarks
O	2020-12-07	First release	Preliminary

CONTENTS

1. GENERAL INFORMATION

No.	Item	Contents	Unit
1	LCD size	7.84 inch (Diagonal)	/
2	Display mode	IPS/Normally black/Transmissive	/
3	Viewing direction(eye)	Free	/
4	Gray scale inversion direction	-	/
5	Resolution(H*V)	1280*400 Pixels	/
6	Module size (L*W*H)	205.78*67.80*4.65	mm
7	Active area (L*W)	190.08*59.40	mm
8	Pixel pitch (L*W)	0.1485*0.1485	mm
9	Interface type	MIPI interface	/
10	Color Depth	16.7M	/
11	Module power consumption	TBD	W
12	Back light type	LED	/
13	Driver IC	NV3051	/
14	Weight	TBD	G

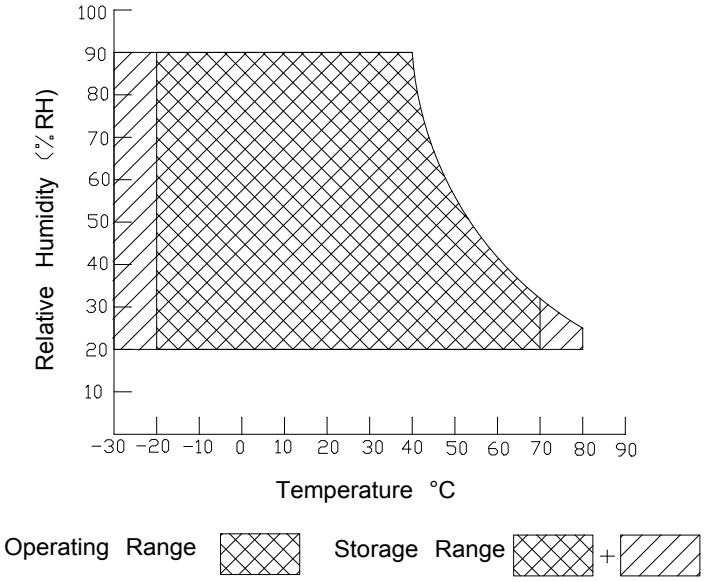
2. ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Min.	Max.	Unit	Note
Power supply input voltage for TFT	VDD	-0.3	5.0	V	
Backlight current (normal temp.)	ILED	-	150	mA	
Operation temperature	Top	-20	+70	°C	Note1
Storage temperature	Tst	-30	+80	°C	Note1
Humidity	RH	-	90%	RH	Note1

Note1 :

1).The relative humidity and temperature range are as below sketch,90%RH Max.

2).The maximum wet bulb temperature ≦40℃ and without dewing.



3. ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS(at Ta=25°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Power supply input voltage	VDD	2.5	2.8	3.6	V	
I/O logic voltage	VDDIO	1.65	1.8	3.6	V	
Input voltage 'H' level	VIH	0.7VDDIO	-	VDDIO	V	
Input voltage 'L' level	VIL	VSS	-	0.3VDDIO	V	
Power supply current	IVDD	-	TBD	-	mA	
TFT gate on voltage	VGH	-	-	-	V	
TFT gate off voltage	VGL	-	-	-	V	
Analog power supply voltage	AVDD	-	-	-	V	
Differential input common mode voltage	Vcom	-	-	-	V	Note1

Note1 : The value is just the reference value. The customer can optimize the setting value by the different D-IC Vcom must be adjusted to optimize display quality, as Crosstalk and Contrast Ratio etc..

4. BACKLIGHT CHARACTERISTICS

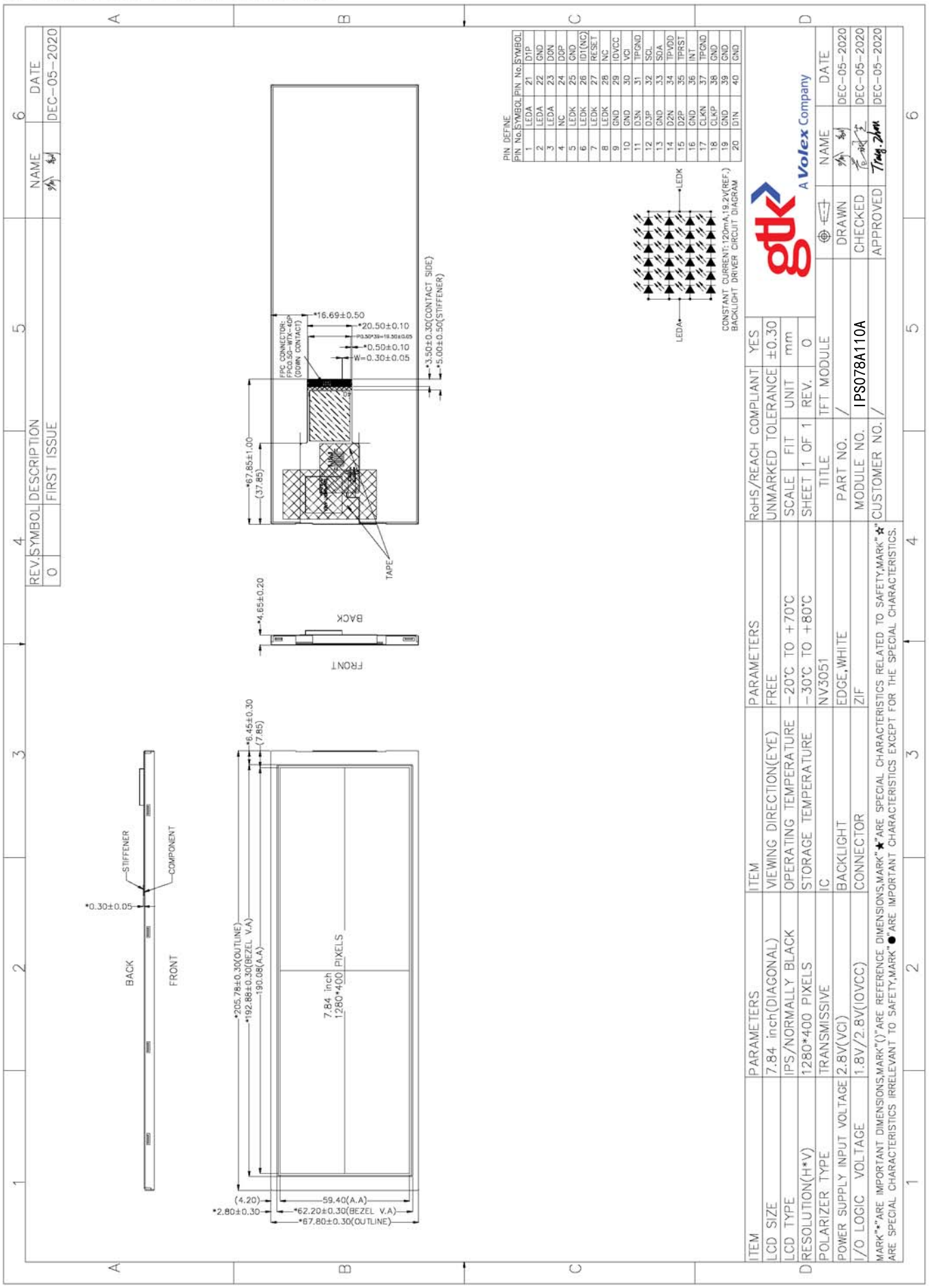
(at Ta=25°C,RH=60%)

Item	Symbol	Min.	Typ.	Max.	Unit	Note
LED forward voltage	VF	16.8	19.2	20.4	V	
LED forward current	IF	-	120	-	mA	IF=30*4mA
LED power consumption	PLED	-	2.304	-	W	Note1
Number of LED	-		24		PCS	
Connection mode	-	6 in series 4 in parallel			/	
LED life-time	-	20000	-	-	Hrs	Note2

Note1 : Calculator value for reference : IF*VF = PLED

Note2 : The LED life-time define as the estimated time to 50% degradation of initial brightness at Ta=25°C and IF =120mA. The LED lifetime could be decreased if operating IF is larger than 120mA.

5. EXTERNAL DIMENSIONS



6. ELECTRO - OPTICAL CHARACTERISTICS

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark	Note
Response time	Tr+ Tf	-	-	30	35	ms	FIG.1	Note 1
Contrast ratio	Cr		700	900	-	-	FIG.2	Note 2
Surface luminance	Lv	θ=0°	400	500	-	cd/m^2	FIG.2	Note 3
Luminance uniformity	Yu	θ=0°	70	80	-	%	FIG.2	Note 4
NTSC	-	θ=0°	-	50	-	%	FIG.2	Note 5
Viewing angle	θ	∅=90°	70	80	-	deg	FIG.3	Note 6
		∅=270°	70	80	-	deg	FIG.3	
		∅=0°	70	80	-	deg	FIG.3	
		∅=180°	70	80	-	deg	FIG.3	
CIE (x,y) chromaticity	Red x	θ=0° ∅=0° Ta=25°C	Typ -0.04	TBD	Typ +0.04	-	FIG.2 CIE1931	Note 5
	Red y			TBD		-		
	Green x			TBD		-		
	Green y			TBD		-		
	Blue x			TBD		-		
	Blue y			TBD		-		
	White x			TBD		-		
	White y			TBD		-		

Note1. Definition of response time

The response time is defined as the LCD optical switching time interval between “White” state and “Black”state.Rise time (T_{ON}) is the time between photo detector output intensity changed from 90% to 10%. And fall time (T_{OFF}) is the time between photo detector output intensity changed from 10% to 90%.
For additional information see FIG1.

Note2.Definition of contrast ratio

Contrast ratio(Cr) is defined mathematically by the following formula.
For more information see FIG.2.

$$\text{Contrast ratio} = \frac{\text{Luminance measured when LCD on the “White” state}}{\text{Luminance measured when LCD on the “Black” state}}$$

Measured at the center area of the LCD

Note3.Definition of surface luminance

Surface luminance is the luminance with all pixels displaying white.
For more information see FIG.2.
Lv = Average Surface Luminance with all white pixels(P1,P2,P3, ...,Pn)

Note4.Definition of luminance uniformity

The luminance uniformity in surface luminance is determined by measuring luminance at each test position 1 through n, and then dividing the maximum luminance of n points luminance by minimum luminance of n points luminance.For more information see FIG.2.

$$Yu = \frac{\text{Minimum surface luminance with all white pixels (P1,P2,P3,.....,Pn)}}{\text{Maximum surface luminance with all white pixels (P1,P2,P3,.....,Pn)}}$$

Note5. Definition of color chromaticity (CIE1931)

CIE (x,y) chromaticity,The x,y value is determined by screen active area center position P5.For more information see FIG.2.

Note6. Definition of viewing angle

Viewing angle is the angle at which the contrast ratio is greater than 10. angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface.
For more information see FIG.3.
For viewing angle and response time testing, the testing data is base on Autronic-Melchers’s ConoScope or DMS series Instruments or compatible. For contrast ratio, Surface Luminance, Luminance uniformity and CIE,the testing data is base on TOPCON’s BM-5or BM-7 photo detector or compatible.

FIG.1. The definition of response Time

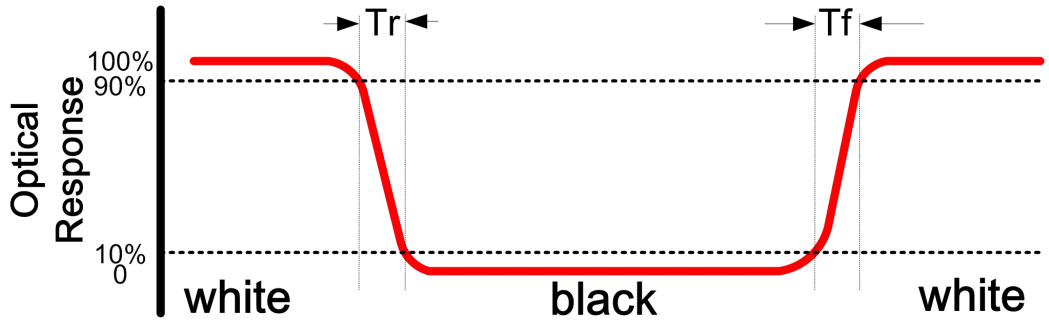


FIG.2. Measuring method for contrast ratio, surface luminance, luminance uniformity, CIE (x,y) chromaticity

H,V : Active area

Light spot size ∅= 5 mm(BM-5) or ∅=7.7mm (BM-7)50cm distance or compatible distance from the LCM surface to detector lens.

Test spot position : see Figure a.

measurement instrument : TOPCON's luminance meter BM-5 or BM-7 or compatible ,see Figure b.

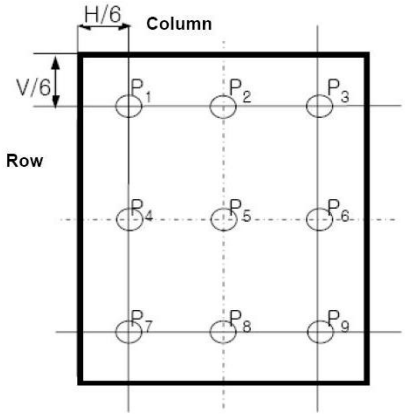


Figure a

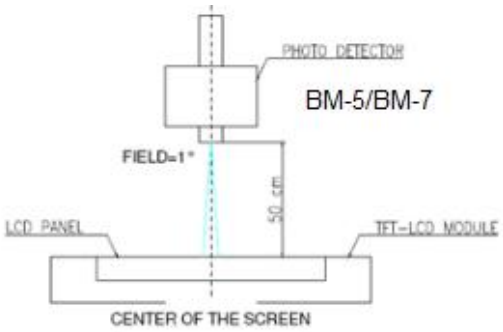
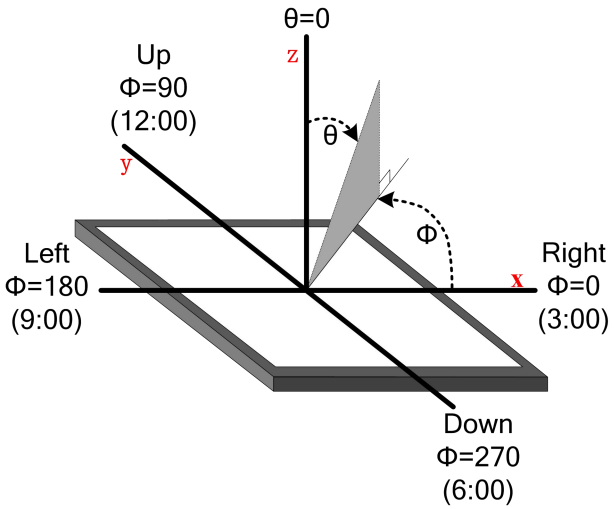


Figure b

FIG.3. The definition of viewing angle



7. INTERFACE DESCRIPTION

Module Interface description

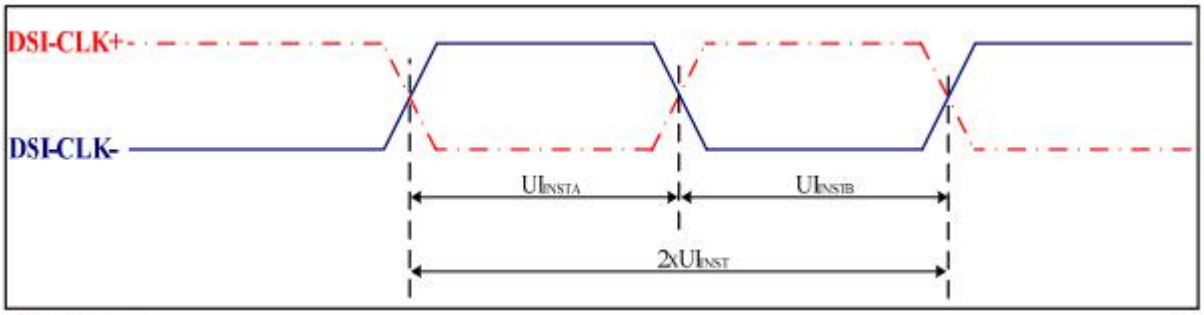
Interface No.	Name	I/O or connect to	Description
1-3	LEDA	I	Anode of Backlight
4	NC	/	Open
5-8	LEDK	I	Cathode of Backlight
9-10	GND	P	Ground
11	D3N	P	MIPI-DSI data Lane 3 negative-end input/output pin
12	D3P	P	MIPI-DSI data Lane 3 positive-end input pin
13	GND	P	Ground
14	D2N	P	MIPI-DSI data Lane negative-end input/output pin
15	D2P	P	MIPI-DSI data Lane positive-end input pin
16	GND	P	Ground
17	CLKN	P	MIPI-DSI clock Lane negative-end input pin
18	CLKP	P	MIPI-DSI clock Lane positive-end input pin
19	GND	P	Ground
20	D1N	P	MIPI-DSI data Lane 1 negative-end input/output pin
21	D1P	P	MIPI-DSI data Lane1 positive-end input pin
22	GND	P	Ground
23	D0N	P	MIPI-DSI data Lane 0 negative-end input/output pin
24	D0P	P	MIPI-DSI data Lane 0 positive-end input pin
25	GND	P	Ground
26	ID1(NC)	/	Open
27	RESET	I	Chip reset signal(“L”->Active)
28	NC	/	Open
29	IOVCC	P	Supply voltage to the interface pins(+1.8V or 2.8V)
30	VCI	P	Supply voltage to the analog circuit (+2.8V)
31	TPGND	P	Ground
32	SCL	I	Serial interface clock
33	SDA	I/O	Serial interface date
34	TPVDD	P	Power of CTP
35	TPRST	I	Reset low
36	INT	O	State change interrupt
37	TPGND	P	Ground
38-40	GND	P	Ground

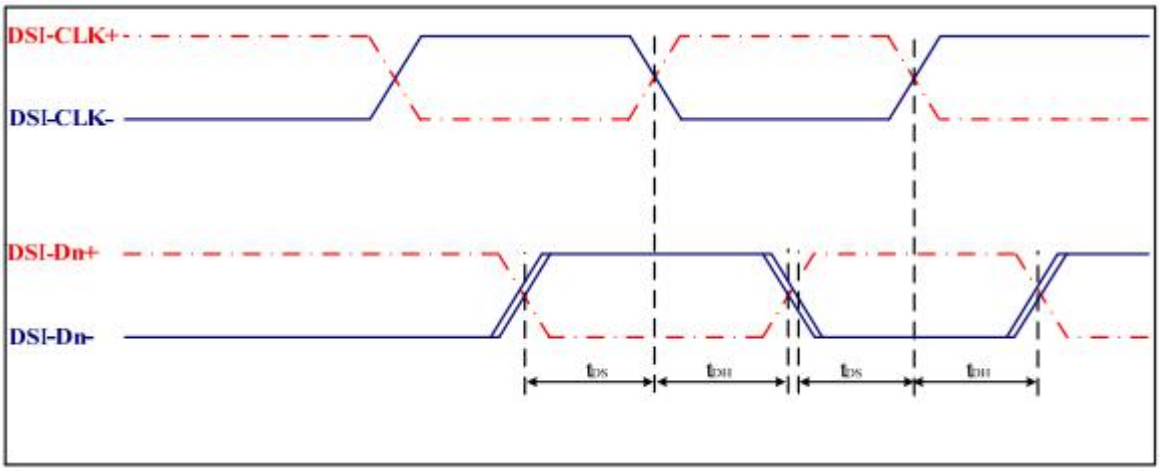
8.AC CHARACTERISTICS

8.1 MIPI-DSI characteristics

8.1.1 High speed mode

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
High Speed Mode						
DSI-CLK+/-	$2Xui_{inst}$	Double UI instantaneous	2.22	-	25	ns
DSI-CLK+/-	UI_{INSTA} , UI_{INSTB}	UI instantaneous Halfs	1.11	-	12.5	ns
DSI-Dn+/-	T_{ds}	Data to clock setup time	0.15	-	-	UI
DSI-Dn+/-	T_{dh}	Data to clock hold time	0.15	-	-	UI
DSI-CLK+/-	T_{drclk}	Differential rise time for clock	150	-	0.3UI	ps
DSI-Dn+/-	T_{drdata}	Differential rise time for data	150	-	0.3UI	ps
DSI-CLK+/-	T_{dfclk}	Differential fall time for clock	150	-	0.3UI	ps
DSI-Dn+/-	T_{dfdata}	Differential fall time for data	150	-	0.3UI	ps





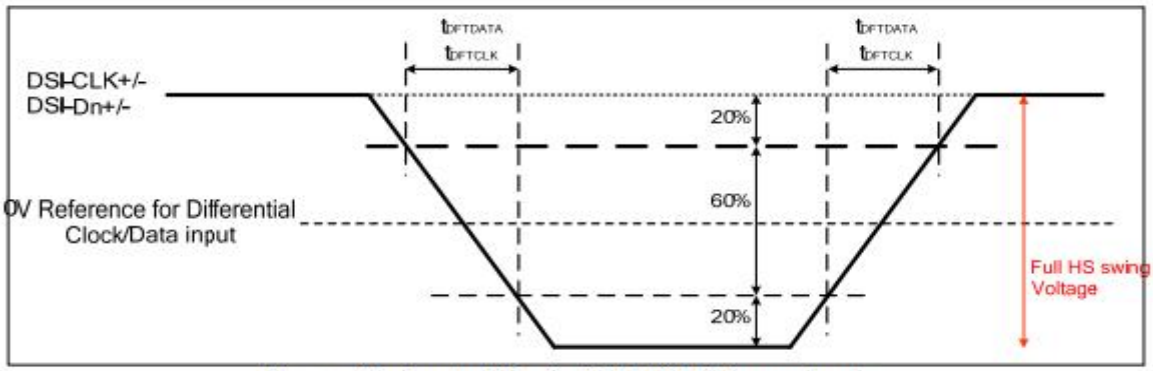


Figure: AC characteristics for MIPI-DSI High speed mode

8.1.2 Low power mode

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
Low Power Mode						
DSI-D0+/-	TLPXM	Length of LP-00, LP-01, LP-10 or LP-11 periods MPU Display Module	50	-	-	ns
DSI- D0+/-	TLPXD	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Modulen MPU	58	-	-	ns
DSI- D0+/-	TTA-SURED	Time-out before the MPU start driving	TLPXD	-	2XTLPXD	ns
DSI- D0+/-	TTA-GETD	Time to drive LP-00 by display module	5XTLPXD	-	-	ns
DSI- D0+/-	TTA-GOD	Time to drive LP-00 after turnaround request – MPU	4XTLPXD	-	-	ns
DSI- D0+/-	Ratio TLPX	Ratio of TLPXM / TLPXD between MCU and display module	2/3	-	3/2	

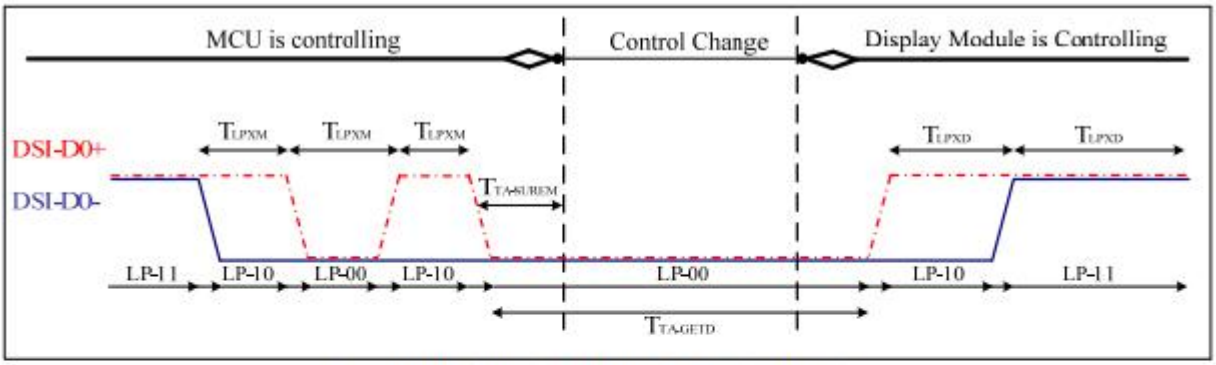


Figure: BTA from the MCU to the Display Module

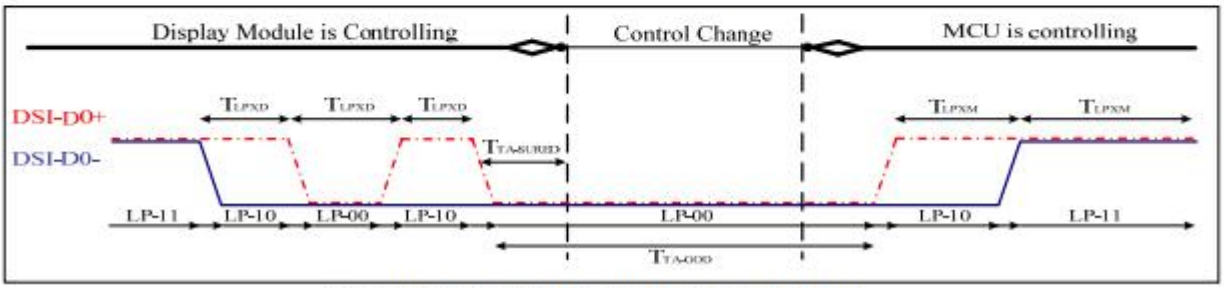


Figure: BTA from the Display Module to the MCU

8.1.3 Bursts

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
High Speed Data Transmission Bursts						
DSI-Dn+/-	TLPX	Length of any low-power state period	50	-	-	ns
DSI- Dn+/-	THS- PREPARE	Time to drive LP-00 to prepare for HS transmission	40ns+4UI	-	85ns+6UI	ns
DSI- Dn+/-	THS-PREPARE+THS-ZERO	THS-PREPARE+time to drive HS-0 before the sync sequence	145ns+10UI	-	-	ns
DSI- Dn+/-	TD-TERM- EN	Time to enable Data Lane receiver line termination measured from when Dn crosses VIL(max)	Time for Dn to reach VTERM-EN	-	35ns+4UI	ns
DSI- Dn+/-	THS-SKIP	Time-out at RX to ignore transition period of EoT	40	-	55ns+4UI	ns
DSI- Dn+/-	THS-TRAIL	Time to drive flipped differential state after last payload data bit of a HS transmission burst	max (8UI, 60ns+4UI)	-	-	ns
DSI- Dn+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	-	-	ns
DSI- Dn+/-	TeoT	Time from start of THS-TRAIL period to start of LP-11 state	-	-	105ns+12UI	ns

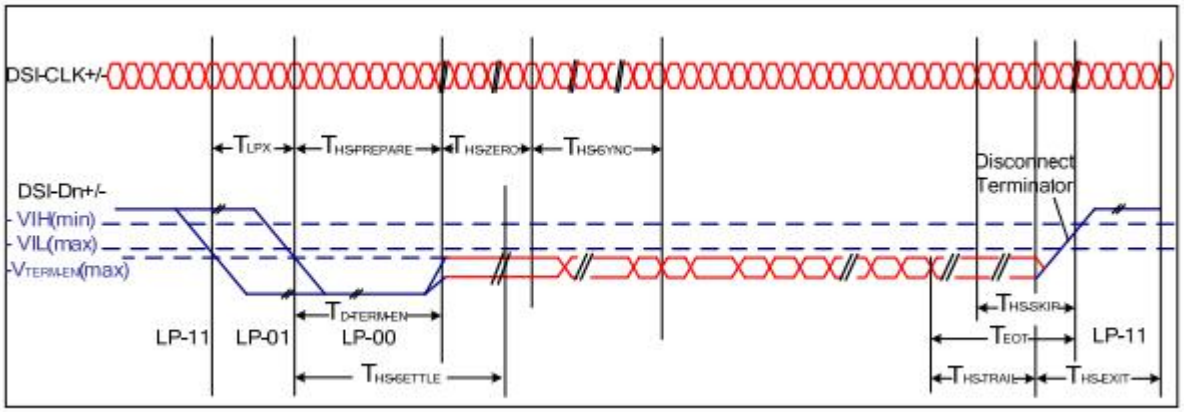


Figure: High Speed Data Transmission Bursts

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
Switching the clock Lane between clock Transmission and Low Power Mode						
DSI-CLK+/-	TCLK-POST	Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	60ns+52UI	-	-	ns
DSI-CLK+/-	TCLK-PRE	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8	-	-	UI
DSI-CLK+/-	TCLK-PREPARE	Time to drive LP-00 to prepare for HS clock transmission	38	-	95	ns
DSI-CLK+/-	TCLK-TERM- EN	Time to enable Clock Lane receiver line termination measured from when Dn crosses $V_{IL(max)}$	Time for Dn to reach VTERM-EN	-	38	ns
DSI- CLK+/-	TCLK-PREPARE +TCLK-ZERO	TCLK-PREPARE + time for lead HS-0 drive period before starting Clock	300	-	-	ns
DSI- CLK+/-	TCLK-TRAIL	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	-	ns
DSI-CLK+/-	TeoT	Time from start of TCLK-TRAIL period to start of LP-11 state	-	-	105ns+ 12UI	ns

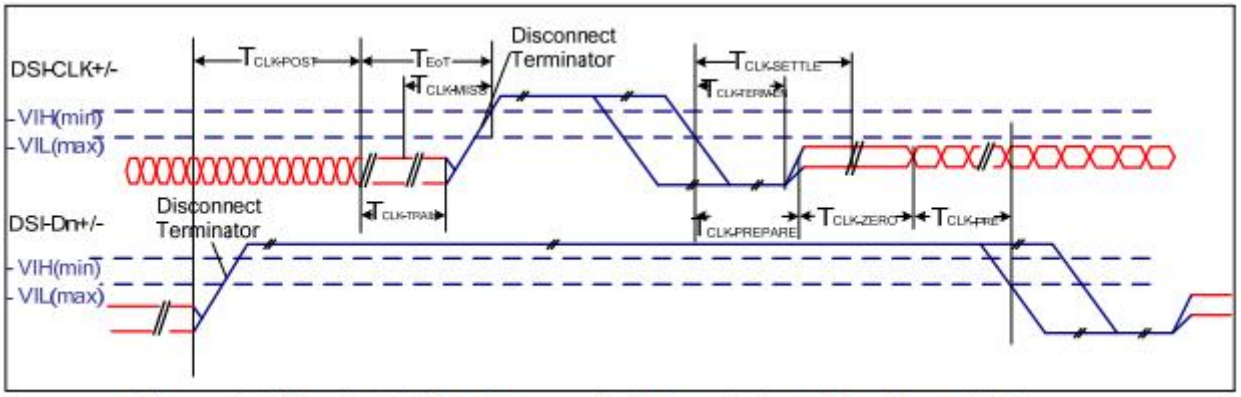
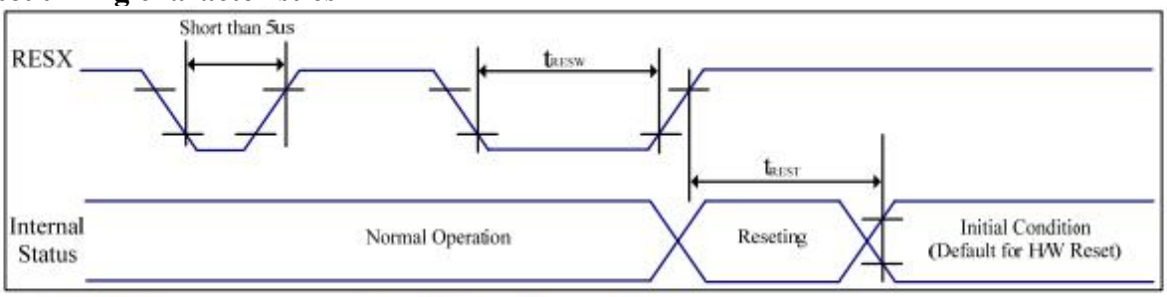


Figure: Switching the clock Lane between clock Transmission and Low Power Mode

8.2 Reset timing characteristics



VSS=0V, IOVCC=1.65V to 3.6V, VCI=2.5V to 6.0V,Ta = -30℃ to 70℃

Symbol	Parameter	Related Pins	MIN	TYP	MAX	Note	Unit
T_{resw}	*1) Reset low pulse width	RESX	10	-	-	-	us
T_{rest}	*2) Reset complete time	-	-	-	5	When reset applied during Sleep in mode	ms
		-	-	-	120	When reset applied during Sleep out mode	ms

Table: Reset input timing

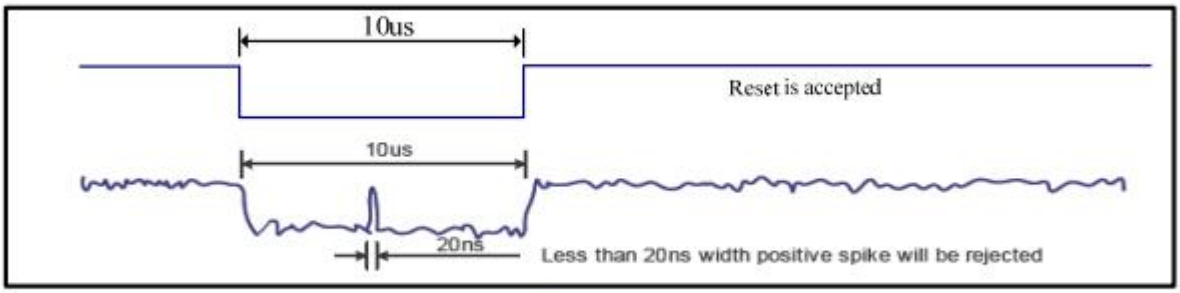
Note 1: Due to an electrostatic discharge on RESX line,spike does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts (It depends on voltage and temperature condition.)

Note 2: During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120ms, when Reset Starts in Sleep Out mode. The display remains the blank state in Sleep In mode) , then return to default condition for H/W reset.

Note 3: During Reset Complete Time, ID1/ID2/ID3 and VCOM value in OTP will be latched to internal register. After a rising edge of RESX, there is a H/W reset complete time (Trest) which lasted 5ms.The loading operation will be done every time during this reset.

Note 4: Spike Rejection also applies during a valid reset pulse as shown below:



Note 5. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120 msec.

9. POWER SEQUENCE

To prevent the device damage from latch up and Improve subjective display effect,the power ON/OFF sequence shown below must be followed.

IOVCC and VCI can be applied in any order. IOVCC and VCI can be powered down in any order.

During power off, if LCD is in the Sleep Out mode, VCI and IOVCC must be powered down minimum 120msec after RESX has been released.

During power off, if LCD is in the Sleep In mode, IOVCC or VCI can be powered down minimum 0msec after RESX has been released.

CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.

Note 1: There will be no damage to the display module if the power sequences are not met.

Note 2: There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.

Note 3: There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command.

Also between receiving Sleep In command and Power Off Sequence.

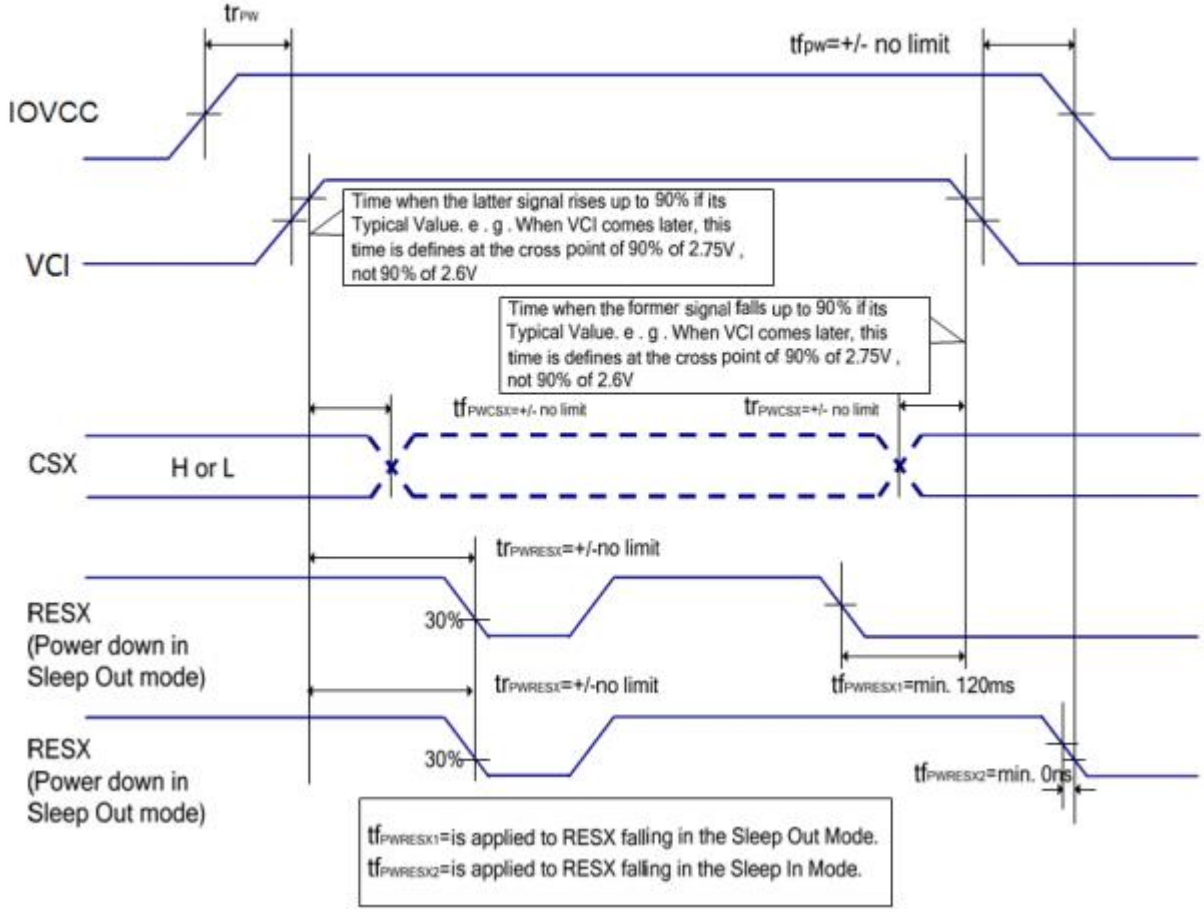
If RESX line is not held stable by host during Power On Sequence, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.

The power on/off sequence is illustrated below:

Case 1 – RESX line is held high or unstable by host at power on

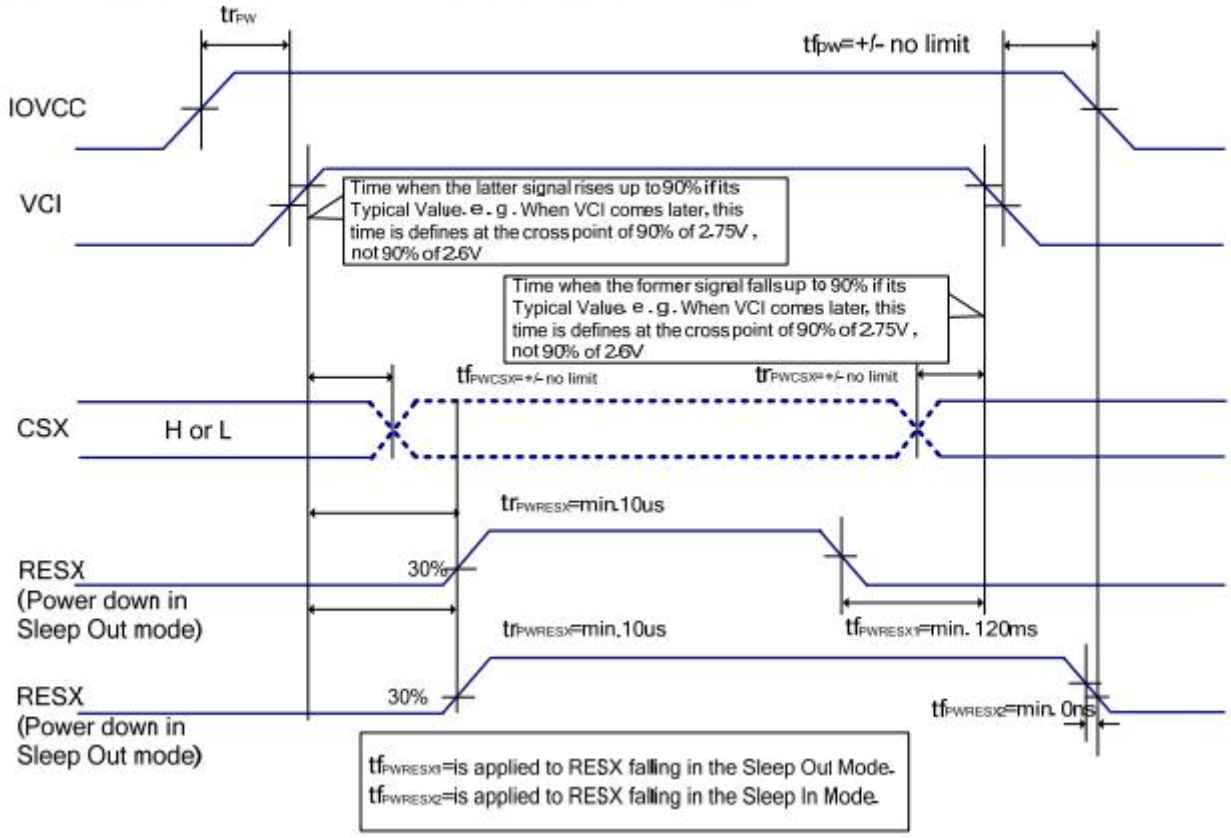
If RESX line is held High or unstable by the host during Power On, then a Hardware Reset must be applied after both VCI and IOVCC have been applied – otherwise correct functionality is not guaranteed.

There is no timing restriction upon this hardware reset.



Case 2 – RESX line is held low or unstable by host at power on

If RESX line is held Low (and stable) by the host during Power On, then the RESX must be held low for minimum 10sec after both VCI and IOVCC have been applied.



Uncontrolled power off

The uncontrolled power off means a situation when e.g. there is removed a battery without the controlled power off sequence. There will not be any damages for the display module or the display module will not cause any damages for the host or lines of the interface.

At an uncontrolled power off the display will go blank and there will not be any visible effects within (TBD) second on the display (blank display) and remains blank until “Power On Sequence” powers it up.

10. RELIABILITY TEST CONDITIONS

No.	Test item	Test condition		Inspection after test
10.1	High temperature storage test	+80°C/240 hours		Inspection after 2~4hours storage at room temperature, the sample shall be free from defects : 1.Current changing value before test and after test is 50% larger; 2. Function defect : Non-display,abnormal-display,missing lines, Short lines,ITO corrosion; 3.Visual defect : Air bubble in the LCD,Seal leak,Glass crack.
10.2	Low temperature storage test	-30°C/240 hours		
10.3	High temperature operating test	+70°C/120 hours		
10.4	Low temperature operating test	-20°C/120 hours		
10.5	Temperature cycle storage test	-30°C ~ 25°C ~ +80°C/10cycles (30min.) (10min.) (30min.)		
10.6	High temperature high humidity test	+50°C*90% RH/120 hours		
10.7	Vibration test	Frequency : 250 r/min Amplitude : 1 inch Time: 45min		
10.8	Drop test	Drop direction: 1 corner/3 edges/6 sides 10 times		
		Packing weight(kg)	Drop height(cm)	
		〈11	80±1.6	
		11≦G〈21	60±1.2	
		21≦G〈31	50±1.0	
		31≦G〈40	40±0.8	
10.9	ESD test	Air discharge: ±8KV, 10times Contact discharge: ±4KV, 10times		

Remark :
1.The test samples should be applied to only one test item.
2.Sample size for each test item is 3~5pcs.
3.For High temperature high humidity test, Pure water(Resistance>10MΩ) should be used.
4.In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judged as a good part.
5.B/L evaluation should be excepted from reliability test with humidity and temperature: Some defects such as black spot/blemish can happen by natural chemical reaction with humidity and Fluorescence B/L has.
6.Failure judgment criterion: Basic specification, Electrical characteristic, Mechanical characteristic, Optical characteristic.
7.After the reliability test, the product only guarantees operation, but don't guarantee all of the cosmetic specification.

11.INSPECTION CRITERION

11.1. Objective

The TFT test criterion are set to formalize TFT quality standards for GTK with reference to those of the customer for inspection, release and acceptance of finished TFT products in order to guarantee the quality of TFT products required by the customer.

11.2. Scope

The criterion is applicable to all the TFT products manufactured by GTK.

11.3. Equipment for Inspection

Electrical tester, electrical testing machines, vernier calipers, microscopes, magnifiers, anti-static wrist straps, finger cots, labels, tri-phase cold and hot shock machine, constant temperature and humidity chamber, backlight table, ovens for high-low temperature experiments, refrigerators, constant voltage power supply (DC）)) , desk Lamps, etc.

11.4. Sampling Plan and Reference Standards

11.4.1.1 Sampling plan:

Refer to National Standard GB/T 2828.1---2012/ISO2859-1:1999，level II of normal levels:

Product Category	Consumer Electronics	Non-consumer Electronics	Industrial	Automobile
AQL	MA=0.4 MI=1.5	MA=0.4 MI=1.0	MA=0.25 MI=0.65	MA=0.15 MI=0.40

11.4.1.2 GB/T 2828.1---2012/ISO2859-1:1999 Sampling check procedure in count

11.4.1.3 GB/T 18910. Standard for LCM parts

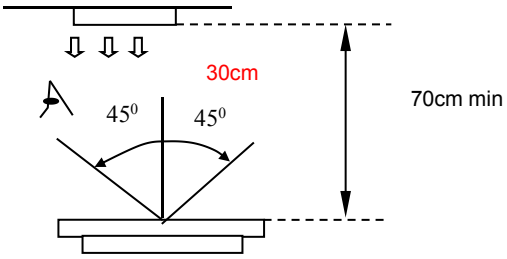
11.4.1.4 GB/T24213-2008 Basic Environmental Test Procedures for Electrical and Electronic Products

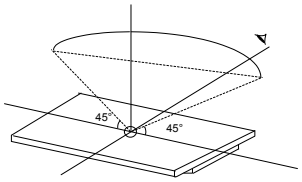
11.4.1.5 IPC-A-610E Acceptability of Electronic Assemblies

11.5. Inspection Conditions and Inspection Reference

11.5.1Cosmetic inspection: shall be done normally at 23±5℃ of the ambient temperature and45~75%RH of relative humidity, under the ambient luminance between 500lux~1000lux and at the distance of 30cm apart between the inspector’s eyes and the LCD panel and normally in reflected light. For backlight LCM, cosmetic inspection shall be done under the ambient luminance less than 100lux with the backlight on.

11.5.2 The TFT shall be tested at the angle of 45°left and right and 0-45° top and bottom as the following picture showing:





11.5.3 Definition of viewing area (VA)

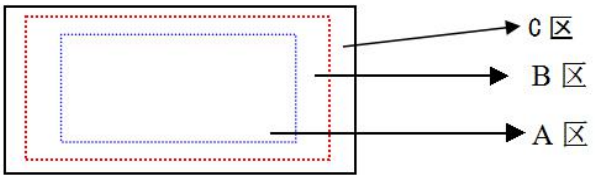
A area：Active area（AA area）

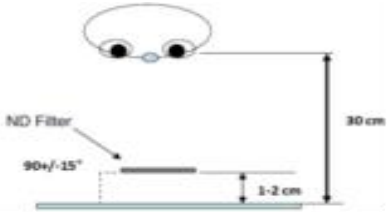
B area: Viewing area（VA area）

C area: Non-viewing area（not viewing after customer assembly）

If there is any appearance viewing defect which do not affect product quality and customer assembly in C area, it’s accepted in generally.

The criteria apply to A and B area except chipping and crack.





11.5.4 Inspection with naked eyes(exclusive of the inspection of the physical dimensions of defects carried out with magnifiers)
11.5.5 ND card use method(refer to right conner image) and scope: Multi-bright dot; Mura(Black/Gray pattern uneven); dark line and so on.
11.5.6 Undefined items or other special items, refer to mutual agreement and limited sample. If criterion does not match product specifications/ technical requirement, both should be subject to special inspection criterion agreed by customer.

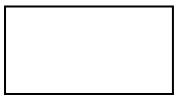
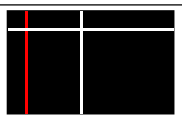
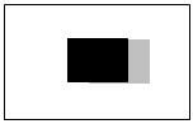
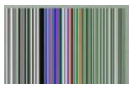
11.6 Defects and Acceptance Standards

11.6.1 Electrical properties test

11.6.1.1 Test voltage(V)：Refer to the instruction of testers and the product specification or drawing and the display content and parameters and display effects shall conform to the product specification and drawing.

11.6.1.2 Current Consumption(I)：Refer to approved product specifications or drawings.

11.6.1.3 Function items(Defect category MA)

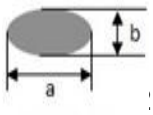
No.	Defects	Descriptions	Pictures	Inspection method/tools	Defect category
11.6.1.3.1	No display /reaction	shows no picture/display in normal connected situation.		Naked eyes/ testers	MA
11.6.1.3.2	Missing segment	Shows missing lines in normal display		Naked eyes/ testers	MA
11.6.1.3.3	Dark line	Only visible on gray pattern, 1 or more vertical/horizontal lines: 5%ND, not visible, OK	/	Naked eyes/ testers	MA
11.6.1.3.4	POL angle defect	Not accepted		Naked eyes/ testers	MA
11.6.1.3.5	Image retention (sticking)	Chess pattern stays for 30mins and change to 50% gray pattern, disappear in 10s, OK; if time>10s, NG		Naked eyes/ testers	MA
11.6.1.3.6	Flicker	Refer to Limit sample if essential or flicker value <-30dB (measured by CA310A); OK		Naked eyes/ CA310A	MA
11.6.1.3.7	Display abnormal	Not accepted		Naked eyes/ testers	MA
11.6.1.3.8	Cross-talk	Refer to limited sample		Naked eyes/ limited sample	MA
11.6.1.3.9	Display dim/bright	Refer to limited sample	/	Naked eyes/ limited sample	MA
11.6.1.3.10	Contrast	Refer to limited sample	/	Naked eyes/ limited sample	MA
11.6.1.3.11	Huge current	Out of spec, not accepted	/	Ammeter	MA
11.6.1.3.12	TP function defect	Not accepted	/	Naked eyes/ Touch/ test program	MA

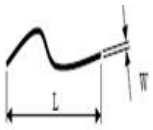
11.6.2 LCD dot/line defect

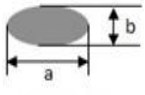
11.6.2.1 LCD pixel dot defect(defect category：MI)

Item	**Inspection criterion**			
Size	S ＜5”	5≤S＜10”	10≤S＜15”	S≥15”
Color pixel dot defect(RGB dot)	1	2	2	3
2 connected bright dot	0	1	1	1
3 connected bright dot or more	0	0	1	0
Bright dot quantity	1	2	3	4
Random dark dot quantity	2	3	4	5
2 connected dark dot	1	1	2	2
3 connected dark dot or more	0	0	0	0
Dark dot quantity	3	4	5	6
Multi-bright dot	ND 5％hidden, OK			
Remark：2 bright dots distance DS≥15mm　2 dark dots distance DS≥5mm 1）Bright dot：Power on TFT and RGB dot in black display 2）Dark dot：Power on TFT and gray or black dot in RGB display 3）Multi-bright dot：Power on TFT and fluorescent tiny dot in black display(only visible in black display)				

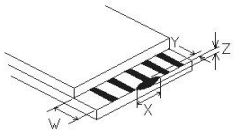
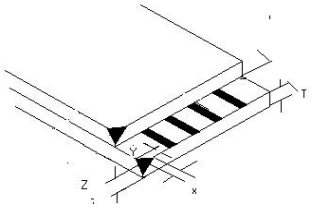
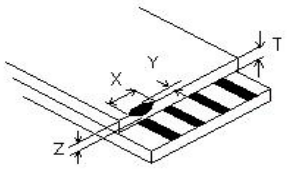
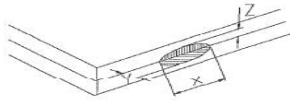
11.6.2.2 LCD appearance dot defect (defect category：MI)

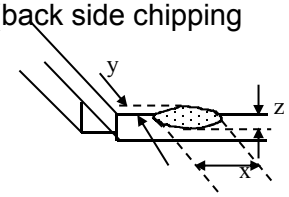
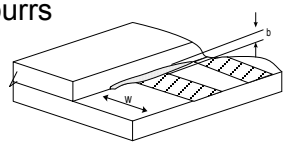
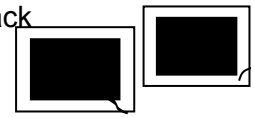
No.	**Item**	**Inspection criterion**					Picture	Inspection method/tools
		Size	S ＜5”	5≤S＜10”	10≤S＜15”	S≥15”		
11.6.2.2.1	Dot defect (black dot, white dot)	D≤0.15	ignore	ignore	D≤0.2; Not count	D≤0.2; ignore		Naked eyes /film card /magnifier
		0.15＜D≤0.25	3	3				
		0.25＜D≤0.30	1	2	0.2~0.35 Q’ty ≤4	0.2~0.35 Q’ty ≤ 5		
		0.30＜D≤0.35	0	1				
		0.35＜D≤0.50	0	0	1	2		
		D＞0.5	0	0	0	0		
		Remark: D≤0.15mm, not count. Multi-dot as bulk is not accepted. Count dot quantity≤ 5; 2 round dots or linear dots in 1 cm is judged as multi-dot.						

No.	Item	Length (mm)	Width (mm)	S ＜5”	5≤S＜10”	10≤S＜15”	S≥15”	Picture	Inspection method/tools
11.6.2.2.2	Line defect (visible when power on)	Not count	W≤0.03	Ignored	Ignored	Ignored	Ignored		Naked eyes /film card /magnifier
		L≤5	0.03≤W＜0.05	3	3	Ignored	Ignored		
		L≤5	0.05≤W＜0.08	0	1	3	3		
		L≤8	0.05≤W＜0.08	0	0	1	2		
		L＞8	W＞0.08	0	0	0	0		
		Remark：Invisible when power on, only visible in special angle against light, show as watermark/folding/scratch but can not be touched, no control or refer to keeping sample.							

11.6.2.2.3	Polarizer convex-concave dot defect, polarizer bubble defect	Size(mm)	S ＜5”	5≤S＜10”	10≤S＜15”	S≥15”		Naked eyes /film card /magnifier
		D≤0.20	Ignored	Ignored	Ignored	Ignored		
		0.20＜D≤0.5	2	2	3	5		
		0.50＜D≤0.8	0	1	2	3		
		0.8＜D≤1.5	0	0	1	2		
		D＞1.5mm	0	0	0	0		

11.6.3 Chipping defect

No.	Item	Accepted criterion(mm)				MAJ	MIN
11.6.3.1	ITO conductive side 	X	/	≤1/8L	/		√
		Y	Y≤1/6W	1/6W <Y≤1/4W	1/4W <Y		
		Accept	2	2	0		
11.6.3.2	Corner chipping (ITOpins position)	X	/	≤1/6L	/		√
		Y	Y≤1/2W	1/2W <Y≤W	W <Y		
		Accept	2	1	0		
		Corner chipping occurred in sealed edge position as per 6.3.3; at the same time it should not enter into black border of the frame and the corner chipping effect the electric connection position perform as per 6.3.1.					
11.6.3.3	Chipping in sealed area (outside chipping)   Chipping in sealed area (inside chipping)	X	/	≤1/8L	/		√
		Y (outside chipping)	Not enter into sealant	Enter Y≤H	H<Y		
		Y (inside chipping)		Enter Y≤1/2H	1/2H<Y		
		Z	≤T	≤1/2T	/		
		Accept	2	1	0		
		The standards of inner and outer chipping on edge sealing area are same. When the chipping occurred in the opposite of stage, Y as per the chipping on the non-conduction side standard in 6.3.1					

11.6.3.4	conductive side (back side chipping  	X	/	≤1/6L	/		√
		Y	Y≤1/3W	1/3W <Y≤2/3W	2/3W <Y		
		Accept	2	2	0		
		Chipping into ITO side ,refer to 6.3.1					
11.6.3.5	Protruding LCD poor cutting and LCD burrs  	X	/	≤1/8L	/		√
		Y	≤1/6W	1/6W <Y≤1/5W	1/5W <Y		
		Z	/	/	/		
		Accept	1	1	1		
		the outside protruding control as per the tolerance of drawing.					
11.6.3.6	Crack 	Not allow to occur cracks without direction; the crack expand to inside is NG, but to outside is OK (confirmed as per the damaged standard)					√
Remark:1)X means the length of chipping; Y means the width; Z means the thickness; W means the step width of the two glasses; H means the distance from the glass edge to the seal inner edge; t means glass thickness.							

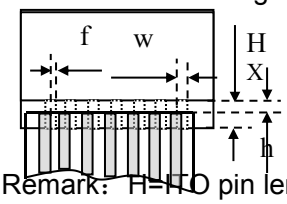
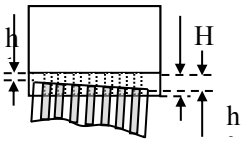
11.6.4 Backlight components

No.	Item	Description	Accepted criterion	MAJ	MIN
11.6.4.1	No backlight wrong Color	/	Rejected	√	
11.6.4.2	Color deviation	When powered on, the LCD color differs from its sample and found that the color not conforming to the drawing after testing.	Refer to sample and drawing.		√
11.6.4.3	Brightness deviation	When powered on, the LCD brightness differs from its sample and is found after testing not conforming to the drawing; or if it conforms to the drawing but the brightness over ±40% than its typical value.	Refer to sample and drawing.		√
11.6.4.4	Uneven brightness	Uneven on the same LCD and out of the specification of the drawing. The no specification evenness= (the max value-the min value)/ mean value< 70%.	Refer to sample and drawing.		√
11.6.4.5	Spot/line /scratch	When power on, it has dirty spot, scratches and so on spot and line defects.	Refer to 6.2.2		√

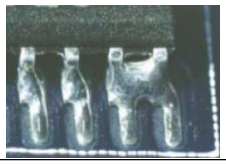
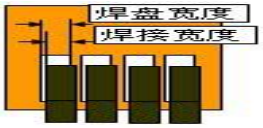
11.6.5 Metal frame (Metal Bezel)

No.	Item	Description	Accepted criterion	MAJ	MIN
11.6.5.1	Material & surface treatment	Metal frame/surface treatment do not conform to the specifications.	Rejected	√	
11.6.5.2	Tab twist Unconformity/ Tab not twisted	Wrong twist method or direction and twist tabs are not twisted as required.	Rejected	√	
11.6.5.3	Bezel paint loss	1.Front surface: Paint peel off and scratch to the bottom Dot:D≤0.5mm, exceeds 3; Line:L≤3.0mm,W≤0.05mm exceeds 2; 2.Front dent, air bubble and side with paint peeling off scratch to the bottom Dot: D≤1.0mm, exceeds 3; Line:L≤10.0mm,W≤0.05mm, exceeds 2;	Rejected		√
11.6.5.4	Bezel scratch				√
11.6.5.5	Painting peel off, discoloration, dent, and scratch				√
11.6.5.6	Burr	Burr(s) on metal bezel is so long as to get into viewing area.	Rejected		√

11.6.6 FPC

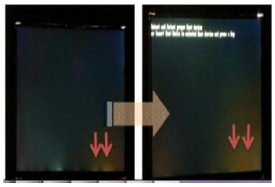
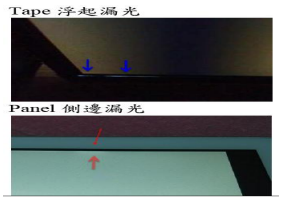
No.	Item	Description	Accepted criterion	MAJ	MIN
11.6.6.1	Model & P/N	Material model & P/N	Keep the same with drawing and technical requirement	√	
11.6.6.2	Dimension/ position	Dimension in drawing spec  Remark: H=ITO pin length f=FPC width W=ITO pin width	f≤1/3w，h ≤1/3H，dimension in drawing spec-> OK Conducive material and ITO/PDA connective area must over than 1/2. Entire dimension must be in spec tolerance.  		√
11.6.6.3	FPC appearance	Hot pressing material get broken, folding line open; FPC golden finger oxidate, broken ,scratch ,foreign material which cause line short	Broken length<2mm; FPC line is OK- > Accepted Crack and line broken-> Rejected		√
11.6.6.4	FPC burr	Burr near FPC edge area	When cover line and burr length ≤1.0mm->Accepted		√
11.6.6.5	FPC falling off	FPC bonding area falling off ; silica gel breaking	Rejected		√
11.6.6.6	Sealant missing ITO line	Sealant is not covered all ITO line	Rejected	√	
11.6.6.7	Missing sealant	No sealant	Rejected	√	
11.6.6.8	Sealant	Sealant height > product total height	Rejected	√	

11.6.7 SMT

No.	Item	Description	Accepted criterion	MAJ	MIN
11.6.7.1	Soldering bridge	Solder between adjacent pads and components 	Rejected		√
11.6.7.2	Solder ball/splash	Solder ball/tin dross causing short circuit at the solder point. There are active solder ball and splash.	Rejected		√
11.6.7.3	Soldering excursion	Soldering slant > 1/3 soldering pad 	Rejected		√
11.6.7.4	Component wrong attaching	Component on PCB differs with drawing: wrong one, extra one, lack one, opposite polarity	Rejected	√	
		JUMP short circuit on PCB: extra soldering ,lack soldering.	Rejected	√	
11.6.7.5	Component falling off	Soldering but component is missing	Rejected	√	
11.6.7.6	Wrong component	Component model/spec differs from product specification	Rejected	√	

11.6.8 General Appearance

No.	Item	Description	Accepted criterion	MAJ	MIN
11.6.8.1	Dimension	According to drawing	Accepted	√	
11.6.8.2	Surface stain	Defect mark or label are not removed residual glue, and finger print,etc;	Rejected		√
11.6.8.3	Assembly foreign material	Dot/linear stain after assembly backlight and diffuse film TP assembly fogy stain	Invisible when power on->OK Refer to 6.2.2 dot/line spec		√
11.6.8.4	Mixture	Different model product in the same shipment	Rejected	√	
11.6.8.5	Product mark	Missing, unclear, incorrect, or misplaced part	Rejected		√
11.6.8.6	Component mark	Silk screen mark clear, resistance measured value in spec	Accepted (Refer to customer special requirement		√
11.6.8.7	Newton's rings	Area<1/6 screen area quantity≤1	Accepted		√

11.6.8.8	Mura	1.In black display ND 5% invisible ->OK; visible->NG 2.Naked eyes inspection RGB display invisible Black display, area<1/4 screen area	Refer to limited sample 		√
11.6.8.9	Light leak	1.LCD edge(near backlight) shadow by LCD lamps irregular illuminate 2.Judge in black/white/gray display (slight leaky is yellowish, greenish, bluefish ->NG）；	Refer to limited sample 		√
11.6.8.10	Polarizer	1.Polarizer slant.Cover VA and not over LCD edge 2.No unmovable stain or finger print in polarizer VA 3.Bubble/warped but not enter VA	Accepted		√
11.6.8.11	TP defect	1.TP crack 2.TP stain(fogy&unremovable) 3.TP glue overflow to VA	Rejected		√

Remark：Anything which is not clearly defined in 6.5~6.8 should refer to IPC-A-610E.Consumer Electronics, Non-consumer Electronics refer to class 1 and Industrial, Automobile refer to Class 2.

11.7. Others

Items not specified in this document or released on compromise should be inspected with reference to mutual agreement and limit samples.

12. HANDLING PRECAUTIONS

12.1 Mounting method

The LCD module consists of two thin glass plates with polarizes which easily be damaged. And since the module in so constructed as to be fixed by utilizing fitting holes in the printed circuit board.
Extreme care should be needed when handling the LCD modules.

12.2 Caution of LCD handling and cleaning

When cleaning the display surface, Use soft cloth with solvent
[recommended below] and wipe lightly :
●.Isopropyl alcohol
●.Ethyl alcohol
Do not wipe the display surface with dry or hard materials that will damage the polarizer surface.
Do not use the following solvent :
●.Water
●.Aromatics
Do not wipe ITO pad area with the dry or hard materials that will damage the ITO patterns
Do not use the following solvent on the pad or prevent it from being contaminated :
●.Soldering flux
●.Chlorine (Cl) , Sulfur (S)
If goods were sent without being silicon coated on the pad, ITO patterns could be damaged due to the corrosion as time goes on.
If ITO corrosion happen by miss-handling or using some materials such as Chlorine (Cl), Sulfur (S) from customer, Responsibility is on customer.

12.3 Caution against static charge

The LCD module use C-MOS LSI drivers, so we recommended that you :
Connect any unused input terminal to Vdd or Vss, do not input any signals before power is turned on, and

ground your body, work/assembly areas, assembly equipment to protect against static electricity.

12.4 Packing

Module employ LCD elements and must be treated as such.

●.Avoid intense shock and falls from a height.

●.To prevent modules from degradation, do not operate or store them exposed direct to sunshine or high temperature/humidity.

12.5 Caution for operation

●.It is an indispensable condition to drive LCD's within the specified voltage limit since the higher voltage then the limit cause the shorter LCD life.

●.An electrochemical reaction due to direct current causes LCD's undesirable deterioration, so that the use of direct current drive should be avoided.

●.Response time will be extremely delayed at lower temperature then the operating temperature range and on the other hand at higher temperature LCD's how dark color in them. However those phenomena do not mean malfunction or out of order with LCD's, which will come back in the specified operation temperature.

●.If the display area is pushed hard during operation, some font will be abnormally displayed but it resumes normal condition after turning off once.

●.A slight dew depositing on terminals is a cause for electro-chemical reaction resulting in terminal open circuit.

●.Usage under the maximum operating temperature, 50%Rh or less is required.

●.When fixed patterns are displayed for a long time,remnant image is likely to occur.

12.6 Storage

In the case of storing for a long period of time for instance, for years for the purpose or replacement use, the following ways are recommended.

●.Storing in an ambient temperature 10°C to 30°C, and in a relative humidity of 45% to 75%. Don't expose to sunlight or fluorescent light.

●.Storing in a polyethylene bag with the opening sealed so as not to enter fresh air outside in it . And with no desiccant.

●.Placing in a dark place where neither exposure to direct sunlight nor light's keeping the storage temperature range.

●.Storing with no touch on polarizer surface by the anything else.

It is recommended to store them as they have been contained in the inner container at the time of delivery from us.

12.7 Safety

●.It is recommendable to crash damaged or unnecessary LCD's into pieces and wash off liquid crystal by either of solvents such as acetone and ethanol, which should be burned up later.

●.When any liquid leaked out of a damaged glass cell comes in contact with your hands, please wash it off well with soap and water.

13. PRECAUTION FOR USE

13.1 A limit sample should be provided by the both parties on an occasion when the both parties agreed its necessity. Judgment by a limit sample shall take effect after the limit sample has been established and confirmed by the both parties.

13.2 On the following occasions, the handing of problem should be decided through discussion and agreement between responsible of the both parties.

●.When a question is arisen in this specification.

●.When a new problem is arisen which is not specified in this specifications.

●.When an inspection specifications change or operating condition change in customer is reported to GTK, and some problem is arisen in this specification due to the change.

●.When a new problem is arisen at the customer's operating set for sample evaluation in the customer site.

14. PACKING SPECIFICATION

Please consult our technical department for detail information.

15. INITIALIZATION CODE

```
#define VBPD      8
#define VFPD      8
#define VSPW      2

#define HBPD     30
#define HFPD     24
#define HSPW     2

#define HDP      400
#define VDP      1280

Wrt_Reg_3051(0xFF,0x30);
Wrt_Reg_3051(0xFF,0x52);
Wrt_Reg_3051(0xFF,0x01);
Wrt_Reg_3051(0xE3,0x00);
Wrt_Reg_3051(0xF6,0xC0);
Wrt_Reg_3051(0xF0,0x00);

Wrt_Reg_3051(0x24,0x08);
Wrt_Reg_3051(0x25,0x0A);

Wrt_Reg_3051(0x28,0xb4);
Wrt_Reg_3051(0x29,0x44);
Wrt_Reg_3051(0x2a,0xff);

Wrt_Reg_3051(0x37,0x74);
Wrt_Reg_3051(0x38,0x7f);
Wrt_Reg_3051(0x39,0x2C);

Wrt_Reg_3051(0x40,0x0E);
Wrt_Reg_3051(0x49,0x3C);
Wrt_Reg_3051(0x59,0xfe);
Wrt_Reg_3051(0x5C,0x00);
Wrt_Reg_3051(0x6D,0x00);
Wrt_Reg_3051(0x6E,0x00);
Wrt_Reg_3051(0x80,0x20);
Wrt_Reg_3051(0x91,0x77);
Wrt_Reg_3051(0x92,0x77);
Wrt_Reg_3051(0x99,0x54);
Wrt_Reg_3051(0x9B,0x56);
Wrt_Reg_3051(0xA0,0x55);
Wrt_Reg_3051(0xA1,0x50);
Wrt_Reg_3051(0xA4,0x9C);

Wrt_Reg_3051(0xA7,0x02);
Wrt_Reg_3051(0xA8,0x01);
Wrt_Reg_3051(0xA9,0x21);
Wrt_Reg_3051(0xAA,0xA8);
Wrt_Reg_3051(0xAB,0x28);
Wrt_Reg_3051(0xAC,0xE0);
Wrt_Reg_3051(0xAD,0xE2);
Wrt_Reg_3051(0xAE,0xE2);
Wrt_Reg_3051(0xAF,0x02);
Wrt_Reg_3051(0xB0,0xE2);
Wrt_Reg_3051(0xB1,0x26);
Wrt_Reg_3051(0xB2,0x28);
Wrt_Reg_3051(0xB3,0x28);
Wrt_Reg_3051(0xB4,0x22);
```

```
Wrt_Reg_3051(0xB5,0xE2);
Wrt_Reg_3051(0xB6,0x26);
Wrt_Reg_3051(0xB7,0xE2);
Wrt_Reg_3051(0xB8,0x26);

Wrt_Reg_3051(0xFF,0x30);
Wrt_Reg_3051(0xFF,0x52);
Wrt_Reg_3051(0xFF,0x02);
Wrt_Reg_3051(0xB1,0x05);
Wrt_Reg_3051(0xD1,0x05);
Wrt_Reg_3051(0xB4,0x2C);
Wrt_Reg_3051(0xD4,0x2A);
Wrt_Reg_3051(0xB2,0x01);
Wrt_Reg_3051(0xD2,0x01);
Wrt_Reg_3051(0xB3,0x29);
Wrt_Reg_3051(0xD3,0x27);
Wrt_Reg_3051(0xB6,0x07);
Wrt_Reg_3051(0xD6,0x05);
Wrt_Reg_3051(0xB7,0x2C);
Wrt_Reg_3051(0xD7,0x2A);
Wrt_Reg_3051(0xC1,0x05);
Wrt_Reg_3051(0xE1,0x05);
Wrt_Reg_3051(0xB8,0x0A);
Wrt_Reg_3051(0xD8,0x0A);
Wrt_Reg_3051(0xB9,0x01);
Wrt_Reg_3051(0xD9,0x01);
Wrt_Reg_3051(0xBD,0x14);
Wrt_Reg_3051(0xDD,0x14);
Wrt_Reg_3051(0xBC,0x12);
Wrt_Reg_3051(0xDC,0x12);
Wrt_Reg_3051(0xBB,0x10);
Wrt_Reg_3051(0xDB,0x10);
Wrt_Reg_3051(0xBA,0x10);
Wrt_Reg_3051(0xDA,0x10);
Wrt_Reg_3051(0xBE,0x17);
Wrt_Reg_3051(0xDE,0x19);
Wrt_Reg_3051(0xBF,0x0E);
Wrt_Reg_3051(0xDF,0x10);
Wrt_Reg_3051(0xC0,0x17);
Wrt_Reg_3051(0xE0,0x19);
Wrt_Reg_3051(0xB5,0x37);
Wrt_Reg_3051(0xD5,0x32);
Wrt_Reg_3051(0xB0,0x02);
Wrt_Reg_3051(0xD0,0x05);

Wrt_Reg_3051(0xFF,0x30);
Wrt_Reg_3051(0xFF,0x52);
Wrt_Reg_3051(0xFF,0x03);
Wrt_Reg_3051(0x00,0x00);
Wrt_Reg_3051(0x01,0x00);
Wrt_Reg_3051(0x02,0x00);
Wrt_Reg_3051(0x03,0x00);
Wrt_Reg_3051(0x08,0x8e);
Wrt_Reg_3051(0x09,0x8e);
Wrt_Reg_3051(0x0A,0x8a);
Wrt_Reg_3051(0x0B,0x89);
Wrt_Reg_3051(0x24,0xf1);
Wrt_Reg_3051(0x25,0xff);
Wrt_Reg_3051(0x30,0x00);
Wrt_Reg_3051(0x31,0x00);
```

```
Wrt_Reg_3051(0x32,0x00);
Wrt_Reg_3051(0x33,0x00);
Wrt_Reg_3051(0x34,0x81);
Wrt_Reg_3051(0x35,0x26);
Wrt_Reg_3051(0x36,0x66);
Wrt_Reg_3051(0x37,0x13);
Wrt_Reg_3051(0x40,0x86);
Wrt_Reg_3051(0x41,0x87);
Wrt_Reg_3051(0x42,0x84);
Wrt_Reg_3051(0x43,0x85);
Wrt_Reg_3051(0x44,0x44);
Wrt_Reg_3051(0x45,0xFF);
Wrt_Reg_3051(0x46,0xFE);
Wrt_Reg_3051(0x48,0x01);
Wrt_Reg_3051(0x49,0x00);
Wrt_Reg_3051(0x50,0x82);
Wrt_Reg_3051(0x51,0x83);
Wrt_Reg_3051(0x52,0x00);
Wrt_Reg_3051(0x53,0x81);
Wrt_Reg_3051(0x55,0x03);
Wrt_Reg_3051(0x56,0x02);
Wrt_Reg_3051(0x58,0x05);
Wrt_Reg_3051(0x59,0x04);
Wrt_Reg_3051(0x60,0x88);
Wrt_Reg_3051(0x61,0x87);

Wrt_Reg_3051(0x80,0x0f);
Wrt_Reg_3051(0x81,0x0E);
Wrt_Reg_3051(0x82,0x0f);
Wrt_Reg_3051(0x88,0x0f);
Wrt_Reg_3051(0x83,0x00);
Wrt_Reg_3051(0x89,0x0e);
Wrt_Reg_3051(0x84,0x06);
Wrt_Reg_3051(0x85,0x07);
Wrt_Reg_3051(0x86,0x04);
Wrt_Reg_3051(0x87,0x05);
Wrt_Reg_3051(0x8A,0x01);
Wrt_Reg_3051(0x8B,0x08);

Wrt_Reg_3051(0x96,0x0f);
Wrt_Reg_3051(0x97,0x0e);
Wrt_Reg_3051(0x98,0x0f);
Wrt_Reg_3051(0x9E,0x0f);
Wrt_Reg_3051(0x99,0x00);
Wrt_Reg_3051(0x9F,0x0e);
Wrt_Reg_3051(0x9A,0x06);
Wrt_Reg_3051(0x9B,0x07);
Wrt_Reg_3051(0x9C,0x04);
Wrt_Reg_3051(0x9D,0x05);
Wrt_Reg_3051(0xA0,0x01);
Wrt_Reg_3051(0xA1,0x08);

Wrt_Reg_3051(0xFF,0x30);
Wrt_Reg_3051(0xFF,0x52);
Wrt_Reg_3051(0xFF,0x02);
Wrt_Reg_3051(0x28,0x0B);
Wrt_Reg_3051(0x29,0x07);
Wrt_Reg_3051(0x2A,0x81);
Wrt_Reg_3051(0x01,0x01);
Wrt_Reg_3051(0x02,0xDA);
```

```
Wrt_Reg_3051(0x03,0xBA);
Wrt_Reg_3051(0x04,0xA8);
Wrt_Reg_3051(0x05,0x9A);
Wrt_Reg_3051(0x06,0x70);
Wrt_Reg_3051(0x07,0xFF);
Wrt_Reg_3051(0x08,0x91);
Wrt_Reg_3051(0x09,0x90);
Wrt_Reg_3051(0x0A,0xFF);
Wrt_Reg_3051(0x0B,0x8F);
Wrt_Reg_3051(0x0C,0x60);
Wrt_Reg_3051(0x0D,0x58);
Wrt_Reg_3051(0x0E,0x48);
Wrt_Reg_3051(0x0F,0x38);
Wrt_Reg_3051(0x10,0x2B);
Wrt_Reg_3051(0xFF,0x30);
Wrt_Reg_3051(0xFF,0x52);
Wrt_Reg_3051(0xFF,0x00);
Wrt_Reg_3051(0x36,0x00);
Wrt_Reg_3051(0x11,0x00);
delay_ms(200);
Wrt_Reg_3051(0x29,0x00);
delay_ms(120);
```

16. HSF COMPLIANCE

●.This products complies with ROHS 2011/65/EU and 2015/863/EU、REACH 1907/2006/EC requirements, and the packaging complies with 94-62-EC.