SPECIFICATION
FOR
TFT MODULE

MODULE NO. :IPS029A110A

CUSTOMER NO. :

Rev No. : O

GTK	PREPARED BY	CHECKED BY	APPROVED BY
SIGNATURE			
DATE	2020.08.31	2020.08.31	2020.08.31

	SIGNATURE	DATE
CUSTOMER APPROVAL		

Notes :

1、Please contact GTK before assigning your product based on this module specification.

2、To improve the quality of product, and this product specification is subject to change without any notice.

REVISION RECORD

Rev No.	Rev date	Contents	Remarks
O	2020-08-31	First release	Preliminary

CONTENTS

1. GENERAL INFORMATION

No.	Item	Contents	Unit
1	LCD size	2.86 inch (Diagonal)	/
2	Display mode	IPS/Normally Black/Transmissive	/
3	Viewing direction(eye)	FREE	/
4	Gray scale inversion direction	-	/
5	Resolution(H*V)	376 *960 Pixels	/
6	Module size (L*W*H)	31.20*76.60*2.14	mm
7	Active area (L*W)	26.51*67.68	mm
8	Pixel pitch (L*W)	0.0705*0.0705	mm
9	Interface type	RGB+SPI / MIPI interface	/
10	Color Depth	16.7M	/
11	Module power consumption	0.37	W
12	Back light type	LED	/
13	Driver IC	ST7701S OR COMPATIBLE	/
14	Weight	11.5	G

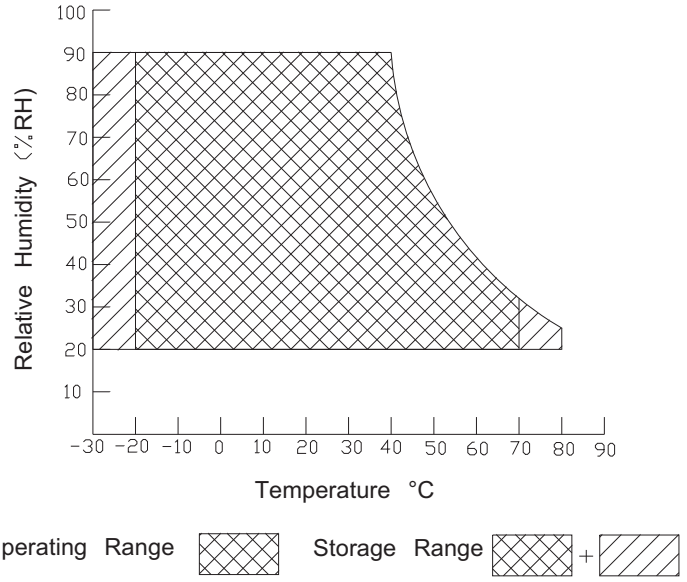
2. ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Min.	Max.	Unit	Note
Power supply input voltage for TFT	VDD	-0.3	4.0	V	
Backlight current (normal temp.)	ILED	-	75	mA	
Operation temperature	Top	-20	+70	°C	Note1
Storage temperature	Tst	-30	+80	°C	Note1
Humidity	RH	20%	90%	RH	Note1

Note1 :

1).The relative humidity and temperature range are as below sketch,90%RH Max.

2).The maximum wet bulb temperature ≦40℃ and without dewing.



3. ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS(at Ta=25°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Power supply input voltage	VDD	2.5	2.8	3.6	V	
I/O logic voltage	VDDIO	1.65	1.8	3.3	V	
Input voltage 'H' level	VIH	0.7VDDIO	-	VDDIO	V	
Input voltage 'L' level	VIL	VSS	-	0.3VDDIO	V	
Power supply current	IVDD	-	40	-	mA	

4. BACKLIGHT CHARACTERISTICS

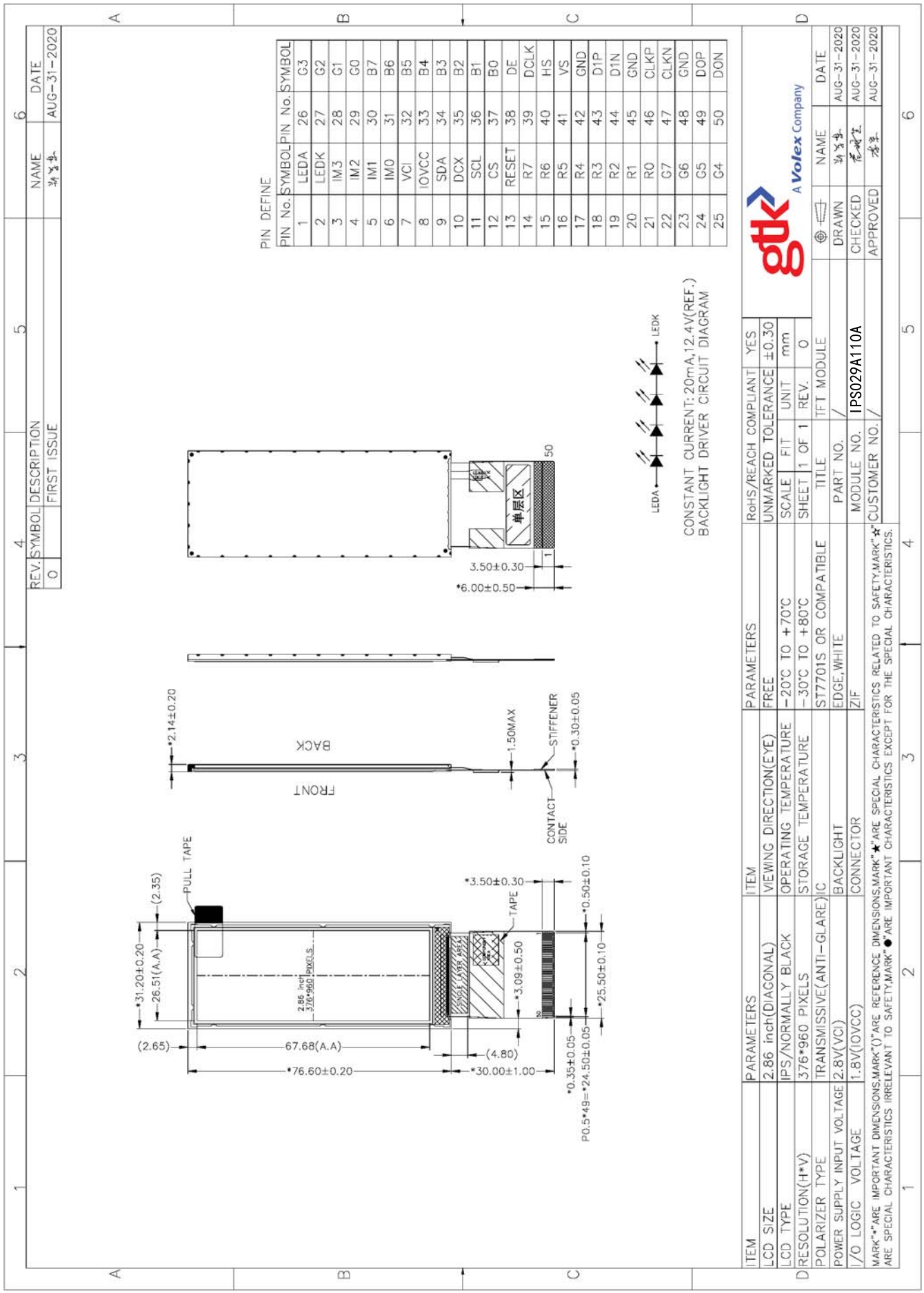
(at Ta=25°C,RH=60%)

Item	Symbol	Min.	Typ.	Max.	Unit	Note
LED forward voltage	VF	11.2	12.4	13.6	V	IF=20mA
LED forward current	IF	-	20	-	mA	
LED power consumption	PLED	-	0.248	-	W	Note1
Number of LED	-		4		PCS	
Connection mode	-	4 in series			/	
LED life-time	-	20000	-	-	Hrs	Note2

Note1 : Calculator value for reference : IF*VF = PLED

Note2 : The LED life-time define as the estimated time to 50% degradation of initial brightness at Ta=25°C and IF =20mA. The LED lifetime could be decreased if operating IF is larger than 20mA.

5. EXTERNAL DIMENSIONS



6. ELECTRO-OPTICAL CHARACTERISTICS

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark	Note
Response time	Tr+ Tf	-	-	30	35	ms	FIG.1	Note 1
Contrast ratio	Cr		800	1000	-	-	FIG.2	Note 2
Surface luminance	Lv	θ=0°	250	300	-	cd/m^2	FIG.2	Note 3
Luminance uniformity	Yu	θ=0°	75	80	-	%	FIG.2	Note 4
NTSC	-	θ=0°	-	50	-	%	FIG.2	Note 5
Viewing angle	θ	∅=90°	-	80	-	deg	FIG.3	Note 6
		∅=270°	-	80	-	deg	FIG.3	
		∅=0°	-	80	-	deg	FIG.3	
		∅=180°	-	80	-	deg	FIG.3	
CIE (x,y) chromaticity	Red x	θ=0° ∅=0° Ta=25°C	Typ -0.04	0.60	Typ +0.04	-	FIG.2 CIE1931	Note 5
	Red y			0.35		-		
	Green x			0.34		-		
	Green y			0.61		-		
	Blue x			0.15		-		
	Blue y			0.07		-		
	White x			0.31		-		
	White y			0.33		-		

Note1. Definition of response time
The response time is defined as the LCD optical switching time interval between “White” state and “Black”state.Rise time (T_{ON}) is the time between photo detector output intensity changed from 90% to 10%. And fall time (T_{OFF}) is the time between photo detector output intensity changed from 10% to 90%.
For additional information see FIG1.

Note2.Definition of contrast ratio
Contrast ratio(Cr) is defined mathematically by the following formula.
For more information see FIG.2.

$$\text{Contrast ratio} = \frac{\text{Luminance measured when LCD on the “White” state}}{\text{Luminance measured when LCD on the “Black” state}}$$

Measured at the center area of the LCD

Note3.Definition of surface luminance
Surface luminance is the luminance with all pixels displaying white.
For more information see FIG.2.
Lv = Average Surface Luminance with all white pixels(P1,P2,P3, ...,Pn)

Note4.Definition of luminance uniformity
The luminance uniformity in surface luminance is determined by measuring luminance at each test position 1 through n, and then dividing the maximum luminance of n points luminance by minimum luminance of n points luminance.For more information see FIG.2.

$$Yu = \frac{\text{Minimum surface luminance with all white pixels (P1,P2,P3,.....,Pn)}}{\text{Maximum surface luminance with all white pixels (P1,P2,P3,.....,Pn)}}$$

Note5. Definition of color chromaticity (CIE1931)
CIE (x,y) chromaticity,The x,y value is determined by screen active area center position P5.For more information see FIG.2.

Note6. Definition of viewing angle
Viewing angle is the angle at which the contrast ratio is greater than 10. angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface.
For more information see FIG.3.
For viewing angle and response time testing, the testing data is base on Autronic-Melchers’s ConoScope or DMS series Instruments or compatible. For contrast ratio, Surface Luminance, Luminance uniformity and CIE,the testing data is base on TOPCON’s BM-5or BM-7 photo detector or compatible.

FIG.1. The definition of response Time

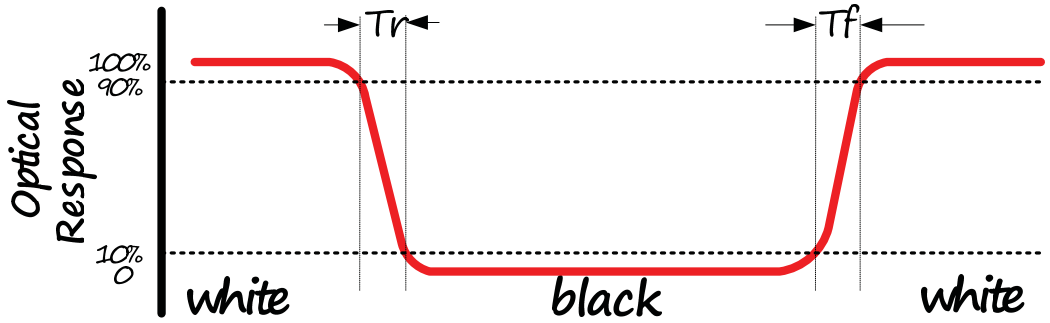


FIG.2. Measuring method for contrast ratio, surface luminance, luminance uniformity, CIE (x,y) chromaticity

H,V : Active area

Light spot size ∅=1.5mm(BM-5) or ∅=7.7mm (BM-7)50cm distance or compatible distance from the LCM surface to detector lens.

Test spot position : see Figure a.

measurement instrument : TOPCON's luminance meter BM-5 or BM-7 or compatible ,see Figure b.

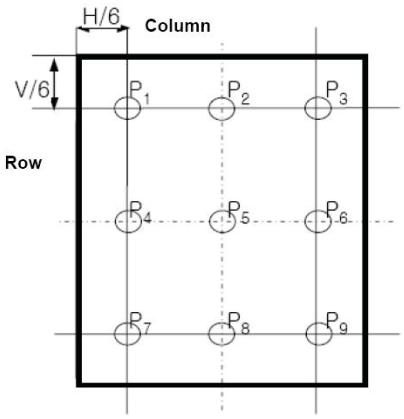


Figure a

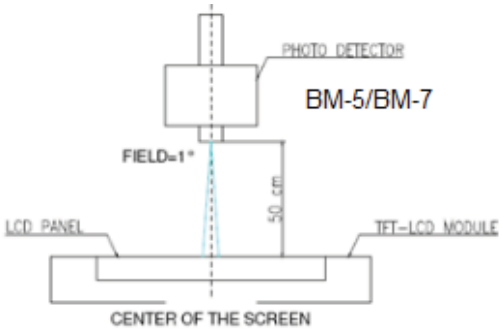
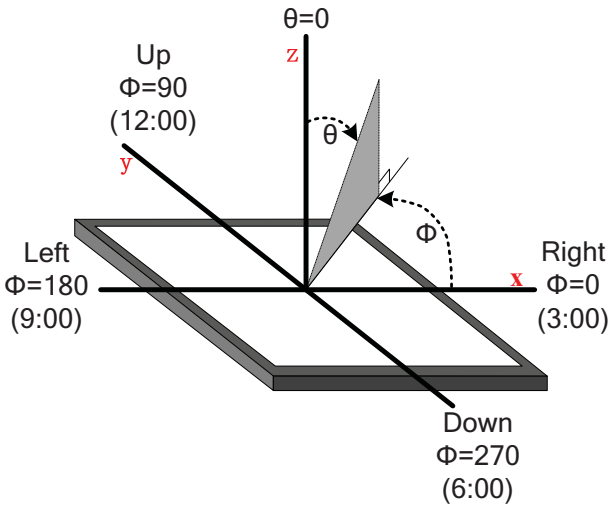


Figure b

FIG.3. The definition of viewing angle



7. INTERFACE DESCRIPTION

Module Interface description

<table>
<tr><th>Interface No.</th><th>Name</th><th>I/O or connect to</th><th>Description</th></tr>
<tr><td>1</td><td>LEDA</td><td>P</td><td>Power for LED backlight(Anode)</td></tr>
<tr><td>2</td><td>LEDK</td><td>P</td><td>Power for LED backlight(Cathode)</td></tr>
<tr><td>3-6</td><td>IM3-IM0</td><td>I</td><td>
<table>
<tr><th>IM3</th><th>IM2</th><th>IM1</th><th>IM0</th><th>MPU Interface Mode</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>RGB+8b_SPI(fall)</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>RGB+9b_SPI(fall)</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>RGB+16b_SPI(rise)</td></tr>
<tr><td>0/1</td><td>1</td><td>0</td><td>1</td><td>MIPI</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>MIPI+16b_SPI(rise)</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>RGB+8b_SPI(rise)</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>RGB+9b_SPI(rise)</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>RGB+16b_SPI(fall)</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>MIPI+16b_SPI(fall)</td></tr>
</table>
</td></tr>
<tr><td>7</td><td>VCI</td><td>P</td><td>Power Supply for Analog</td></tr>
<tr><td>8</td><td>IOVCC</td><td>P</td><td>Power Supply for I/O System.</td></tr>
<tr><td>9</td><td>SDA</td><td>I/O</td><td>Serial in/out signal.</td></tr>
<tr><td>10</td><td>DCX</td><td>I</td><td>Data/ Command selection pin.
Low :Command
High: Parameter</td></tr>
<tr><td>11</td><td>SCL</td><td>I</td><td>SCL:As serial clock when operate in the serial interface</td></tr>
<tr><td>12</td><td>CS</td><td>I</td><td>Chip select input signal.
Low:The chip is selected and accessible
High:The chip is not selected and not accessible</td></tr>
<tr><td>13</td><td>RESET</td><td>I</td><td>The external reset input
Initializes the chip with a low input. Be sure to execute a power-on
reset after supplying power.</td></tr>
<tr><td>14-21</td><td>R7-R0</td><td>I</td><td rowspan="3">A 24-bit parallel data bus for RGB Interface.
24-bit/pixel: D[23:16]=R,D[15:8]=G,D[7:0]=B
18-bit/pixel: MDT=0:D[21:16]=R,D[13:8]=G,D[5:0]=B
MDT=1:D[17:12]=R,D[11:6]=G,D[5:0]=B
16-bit/pixel: D[20:16]=R,D[13:8]=G,[4:0]=B</td></tr>
<tr><td>22-29</td><td>G7-G0</td><td>I</td></tr>
<tr><td>30-37</td><td>B7-B0</td><td>I</td></tr>
<tr><td>38</td><td>DE</td><td>I</td><td>Data enable signal for RGB interface operation.</td></tr>
<tr><td>39</td><td>DCLK</td><td>I</td><td>Dot clock signal for RGB interface operation.</td></tr>
<tr><td>40</td><td>HS</td><td>I</td><td>Line synchronizing signal for RGB interface operation.</td></tr>
<tr><td>41</td><td>VS</td><td>I</td><td>Frame synchronizing signal for RGB interface operation.</td></tr>
<tr><td>42</td><td>GND</td><td>P</td><td>Ground</td></tr>
<tr><td>43</td><td>D1P</td><td>I</td><td>Low voltage differential clock signal</td></tr>
<tr><td>44</td><td>D1N</td><td>I</td><td>Low voltage differential clock signal</td></tr>
<tr><td>45</td><td>GND</td><td>P</td><td>Ground</td></tr>
<tr><td>46</td><td>CLKP</td><td>I</td><td>Low voltage differential data signal</td></tr>
<tr><td>47</td><td>CLKN</td><td>I</td><td>Low voltage differential data signal</td></tr>
<tr><td>48</td><td>GND</td><td>P</td><td>Ground</td></tr>
<tr><td>49</td><td>D0P</td><td>I</td><td>Low voltage differential data signal</td></tr>
<tr><td>50</td><td>D0N</td><td>I</td><td>Low voltage differential data signal</td></tr>
</table>

8.AC CHARACTERISTICS

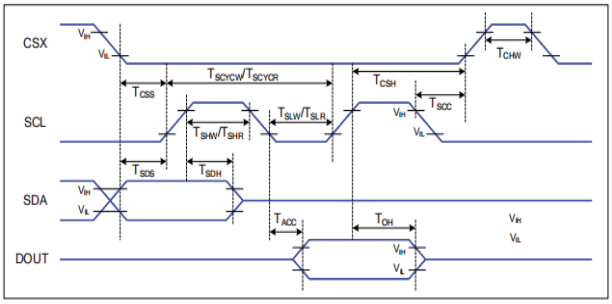


Figure 1 3-line serial Interface Timing Characteristics

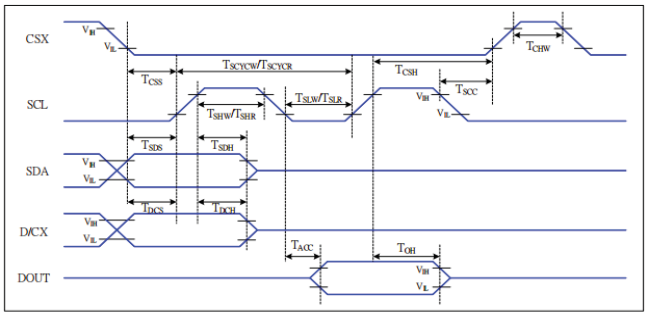


Figure 2 4-line serial Interface Timing Characteristics

VDDI=1.8,VDD=2.8, AGND=DGND=0V, Ta=25℃

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	60		ns	
	T_{CHW}	Chip select "H" pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	66		ns	
	T_{SHW}	SCL "H" pulse width (Write)	15		ns	
	T_{SLW}	SCL "L" pulse width (Write)	15		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	
	T_{SHR}	SCL "H" pulse width (Read)	60		ns	
	T_{SLR}	SCL "L" pulse width (Read)	60		ns	
SDA (DIN)	T_{SDS}	Data setup time	10		ns	
	T_{SDH}	Data hold time	10		ns	

Table 4 3-line serial Interface Characteristics

Note : The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select "H" pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	66		ns	-write command & data ram
	T_{SHW}	SCL "H" pulse width (Write)	15		ns	
	T_{SLW}	SCL "L" pulse width (Write)	15		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	-read command & data ram
	T_{SHR}	SCL "H" pulse width (Read)	60		ns	
	T_{SLR}	SCL "L" pulse width (Read)	60		ns	
D/CX	T_{DCS}	D/CX setup time	10		ns	
	T_{DCH}	D/CX hold time	10		ns	
SDA (DIN)	T_{SDS}	Data setup time	10		ns	
	T_{SDH}	Data hold time	10		ns	

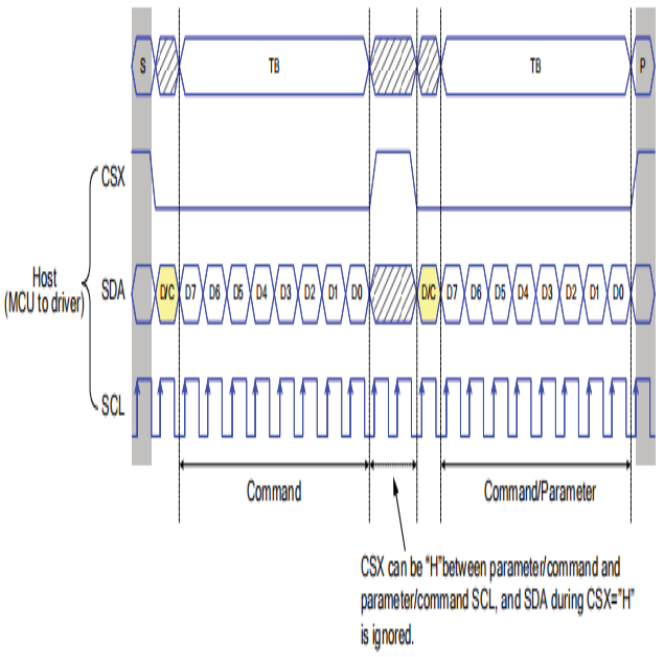


Figure 11 3-line serial interface write protocol (write to register with control bit in transmission)

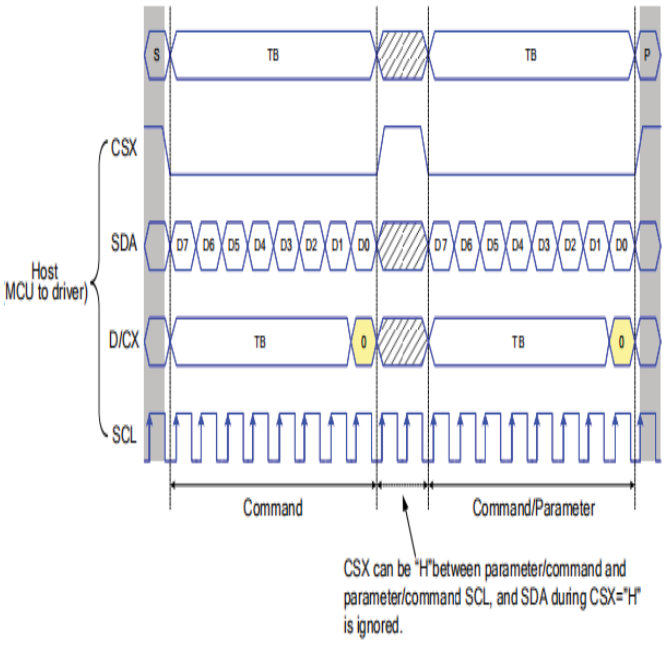


Figure 12 4-line serial interface write protocol (write to register with control bit in transmission)

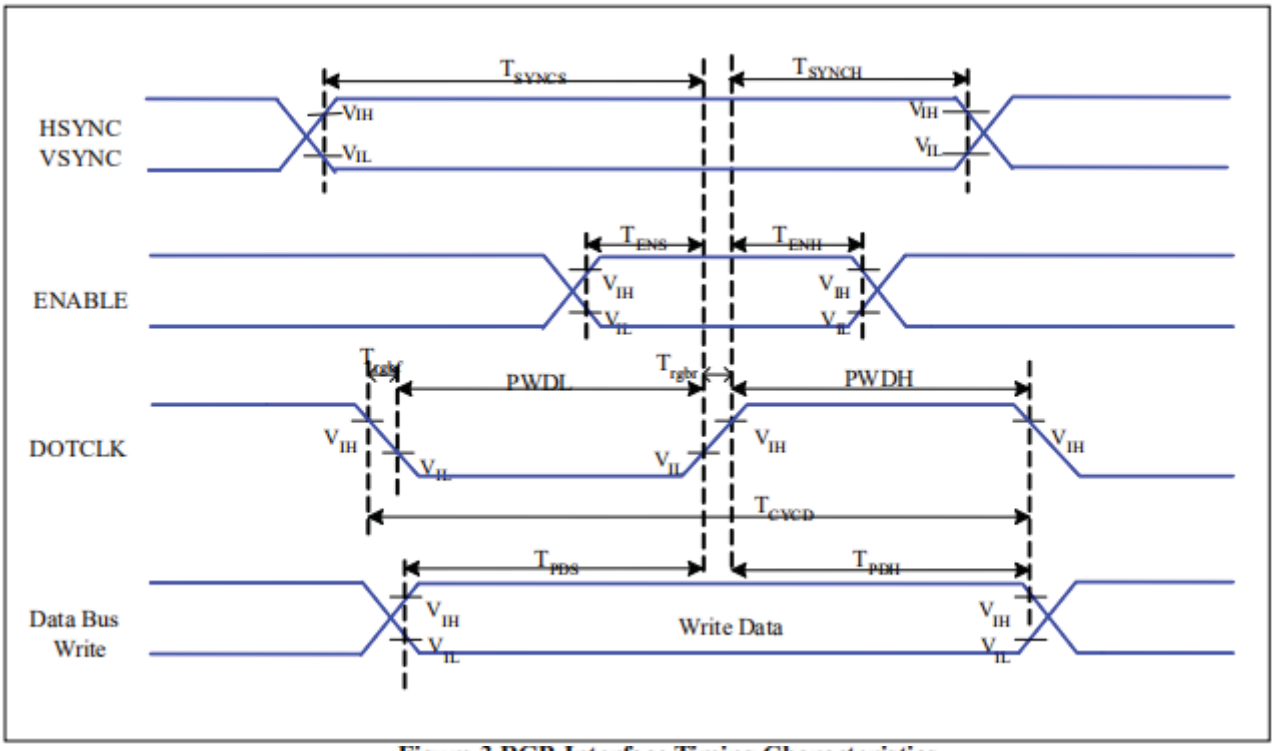


Figure 3 RGB Interface Timing Characteristics

VDDI=1.8,VDD=2.8, AGND=DGND=0V, Ta=25 ℃

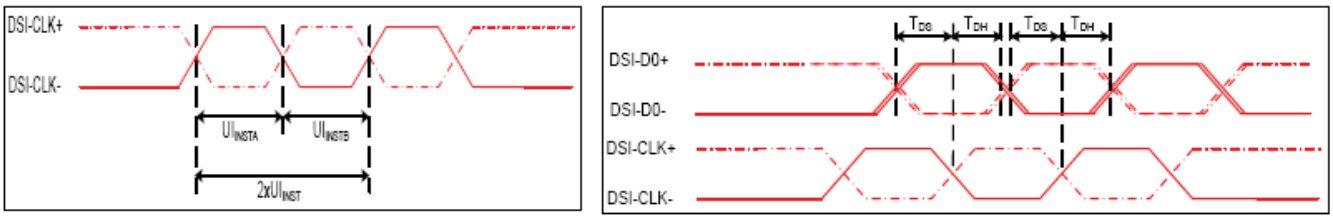
Signal	Symbol	Parameter	MIN	MAX	Unit	Description
HSYNC, VSYNC	T_{SYNCS}	VSYNC, HSYNC Setup Time	5	-	ns	
ENABLE	T_{ENS}	Enable Setup Time	5	-	ns	
	T_{ENH}	Enable Hold Time	5	-	ns	
DOTCLK	PWDH	DOTCLK High-level Pulse Width	15	-	ns	
	PWDL	DOTCLK Low-level Pulse Width	15	-	ns	
	T_{CYCD}	DOTCLK Cycle Time	33	-	ns	
	Trghr, Trghf	DOTCLK Rise/Fall time	-	15	ns	
DB	T_{PDS}	PD Data Setup Time	5	-	ns	
	T_{PDH}	PD Data Hold Time	5	-	ns	

Please refer to the following table for the setting limitation of RGB interface signals.

Parameter	Symbol	Min.	Typ.	Max.	Unit
Horizontal Sync. Width	hpw	2	-	255	Clock
Horizontal Sync. Back Porch	hbp	2	--	255	Clock
Horizontal Sync. Front Porch	hfp	2	--	-	Clock
Vertical Sync. Width	vs	2	--	254	Line
Vertical Sync. Back Porch	vbp	2	--	254	Line
Vertical Sync. Front Porch	vfp	2	--	--	Line

1. *Typical value are related to the setting frame rate is 60Hz..*

High Speed Mode

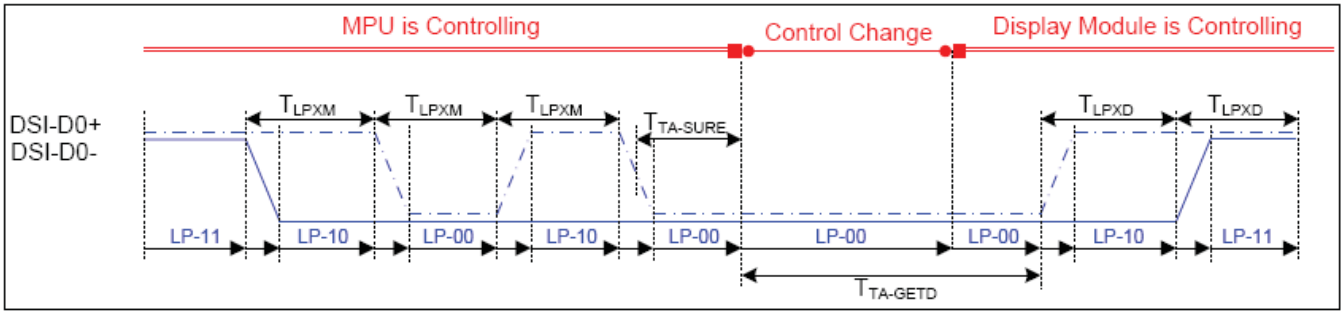


DSI clock channel timing

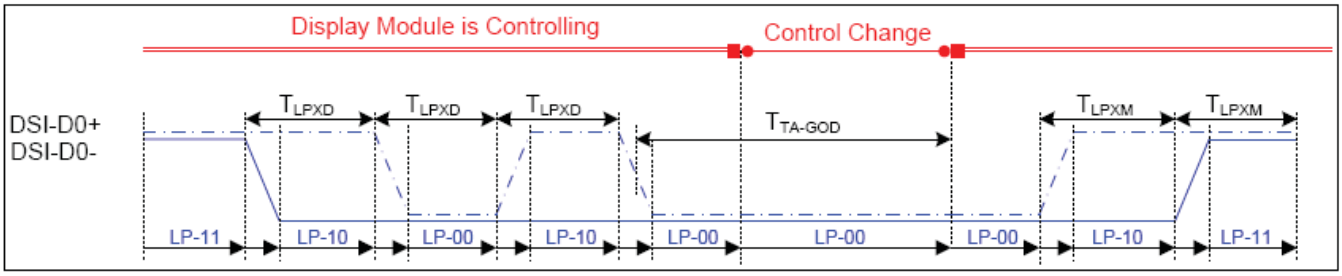
VDDI=1.8,VDD=2.8, AGND=DGND=0V, Ta=25 ℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
DSI-CLK+/-	$2xUI_{INSTA}$	Double UI instantaneous	4	25	ns	
DSI-CLK+/-	UI_{INSTA} UI_{INSTB}	UI instantaneous halfs	2	12.5	ns	$UI = UI_{INSTA} = UI_{INSTB}$
DSI-Dn+/-	tDS	Data to clock setup time	0.15	-	UI	
DSI-Dn+/-	tDH	Data to clock hold time	0.15	-	UI	

Lowe Power Mode



Bus Turnaround (BTA) from display module to MPU Timing

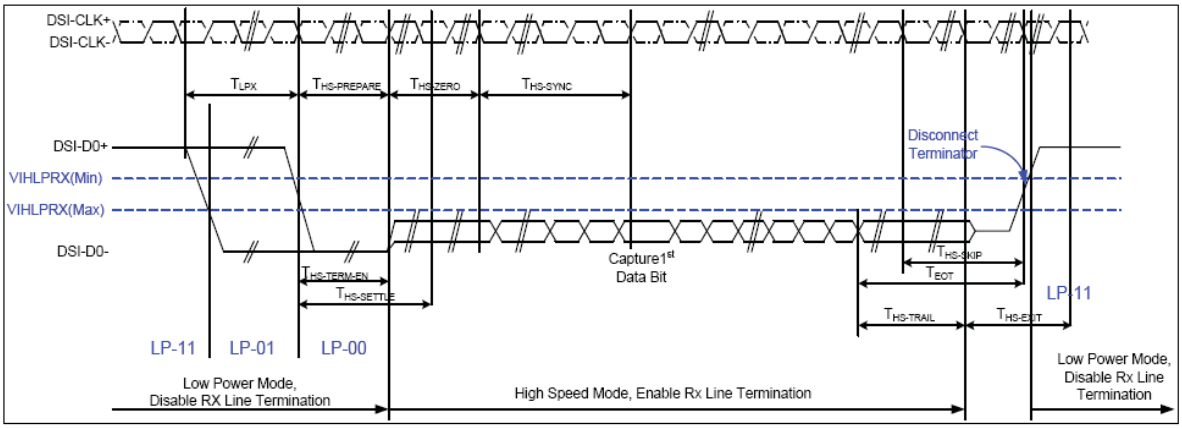


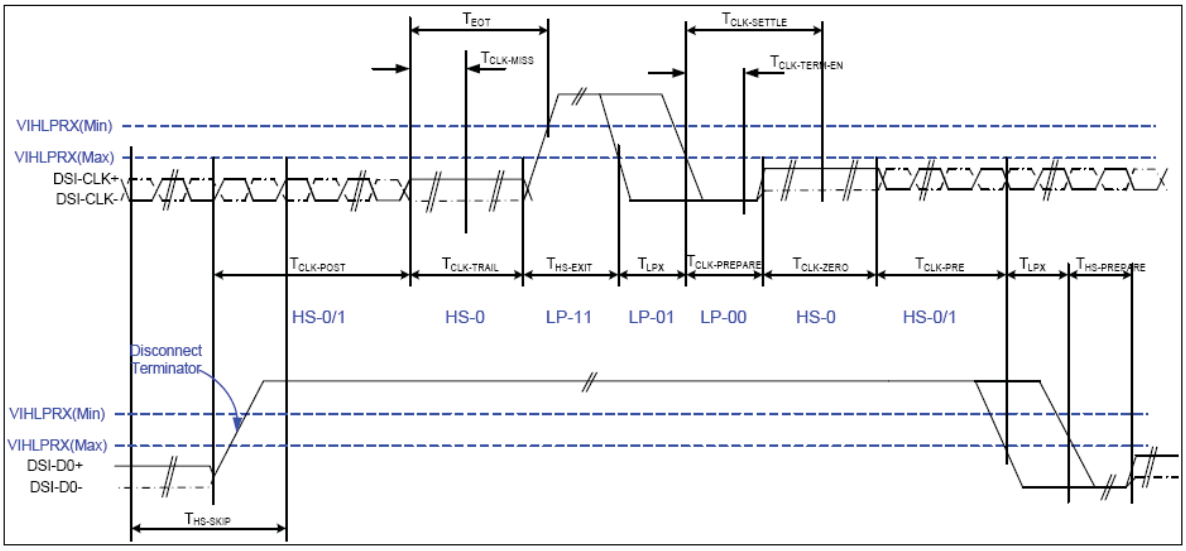
Bus Turnaround (BTA) from MPU to display module Timing

VDDI=1.8,VDD=2.8, AGND=DGND=0V, Ta=25 ℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
DSI-D0+/-	TLPXM	Length of LP-00,LP-01, LP-10 or LP-11 periods MPU→Display Module	50	75	ns	Input
DSI-D0+/-	TLPXD	Length of LP-00,LP-01, LP-10 or LP-11 periods MPU→Display Module	50	75	ns	Output
DSI-D0+/-	TTA-SURED	Time-out before the MPU start driving	T_{LPXD}	$2xT_{LPXD}$	ns	Output
DSI-D0+/-	TTA-GETD	Time to drive LP-00 by display module	$5xT_{LPXD}$		ns	Input
DSI-D0+/-	TTA-GOD	Time to drive LP-00 after turnaround request-MPU	$4xT_{LPXD}$		ns	Output

DSI Bursts Mode

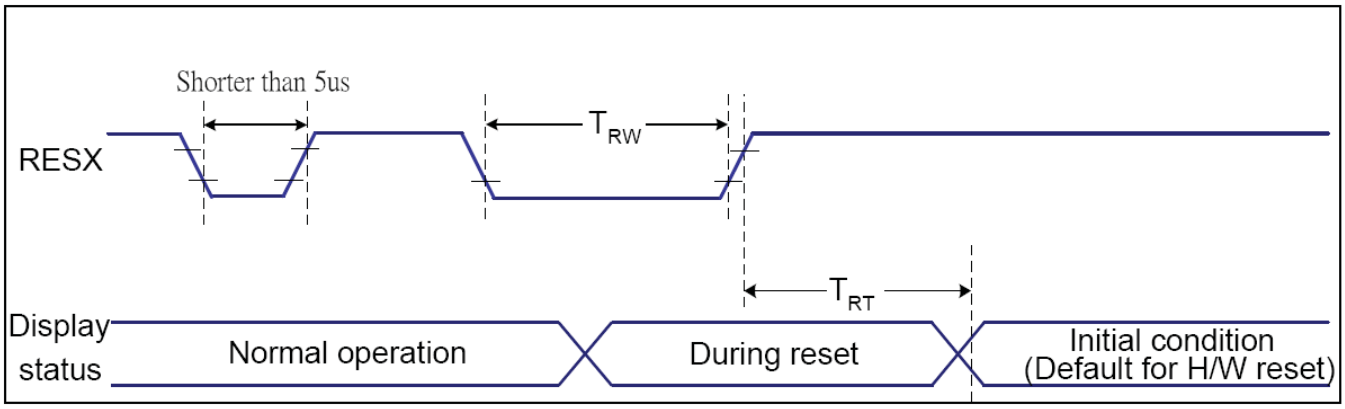




VDDI=1.8,VDD=2.8, AGND=DGND=0V, Ta=25 ℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
Low Power Mode to High Speed Mode Timing						
DSI-Dn+/-	TLPX	Length of any low power state period	50	-	ns	Input
DSI-Dn+/-	THS-PREPARE	Time to drive LP-00 to prepare for HS transmission	40+4 UI	85+6 UI	ns	Input
DSI-Dn+/-	THS-TERM-EN	Time to enable data receiver line termination measured from when Dn crosses VILMAX	-	35+4 UI	ns	Input
DSI-Dn+/-	THS-PREPARE + THS-ZERO	THS-PREPARE + time to drive HS-0 before the sync sequence	140+ 10UI	-	ns	Input
High Speed Mode to Low Power Mode Timing						
DSI-Dn+/-	THS-SKIP	Time-out at display module to ignore transition period of EoT	40	55+4 UI	ns	Input
DSI-Dn+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	-	ns	Input
DSI-Dn+/-	THS-TRAIL	Time to drive flipped differential state after last payload data bit of a HS transmission burst	60+4 UI	-	ns	Input
High Speed Mode to/from Low Power Mode Timing						
DSI-CLK+/-	TCLK-POS	Time that the MPU shall continue sending HS clock after the last associated data lane has transition to LP mode	60+5 2UI	-	ns	Input
DSI-CLK+/-	TCLK-TRAIL	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns	Input
DSI-CLK+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	-	ns	Input
DSI-CLK+/-	TCLK-PREPARE	Time to drive LP-00 to prepare for HS transmission	38	95	ns	Input
DSI-CLK+/-	TCLK-TERM-EN	Time-out at clock lan display module to enable HS transmission	--	38	ns	Input
DSI-CLK+/-	TCLK-PREPARE + TCLK-ZERO	Minimum lead HS-0 drive period before starting clock	300	-	ns	Input
DSI-CLK+/-	TCLK-PRE	Time that the HS clock shall be driven prior to any associated data lane beginning the transition from LP to HS mode	8UI	-	ns	Input
DSI-CLK+/-	TEOT	Time form start of TCLK-TRAIL period to start of LP-11 state	-	105n s+12 UI	ns	Input

Reset Timing:



VDDI=1.8,VDD=2.8, AGND=DGND=0V, Ta=25 ℃

Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1, 5)	ms
				120(Note 1, 6, 7)	ms

Notes:

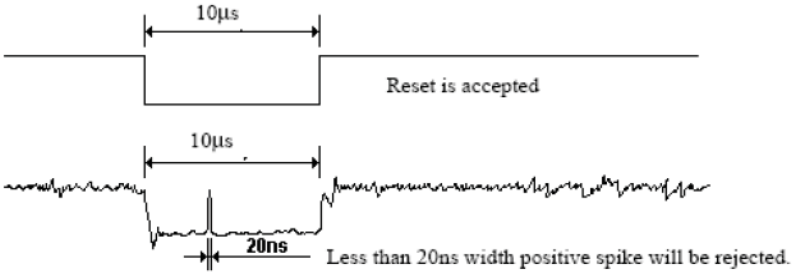
1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.

6. When Reset applied during Sleep Out Mode.

7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

9. POWER SEQUENCE

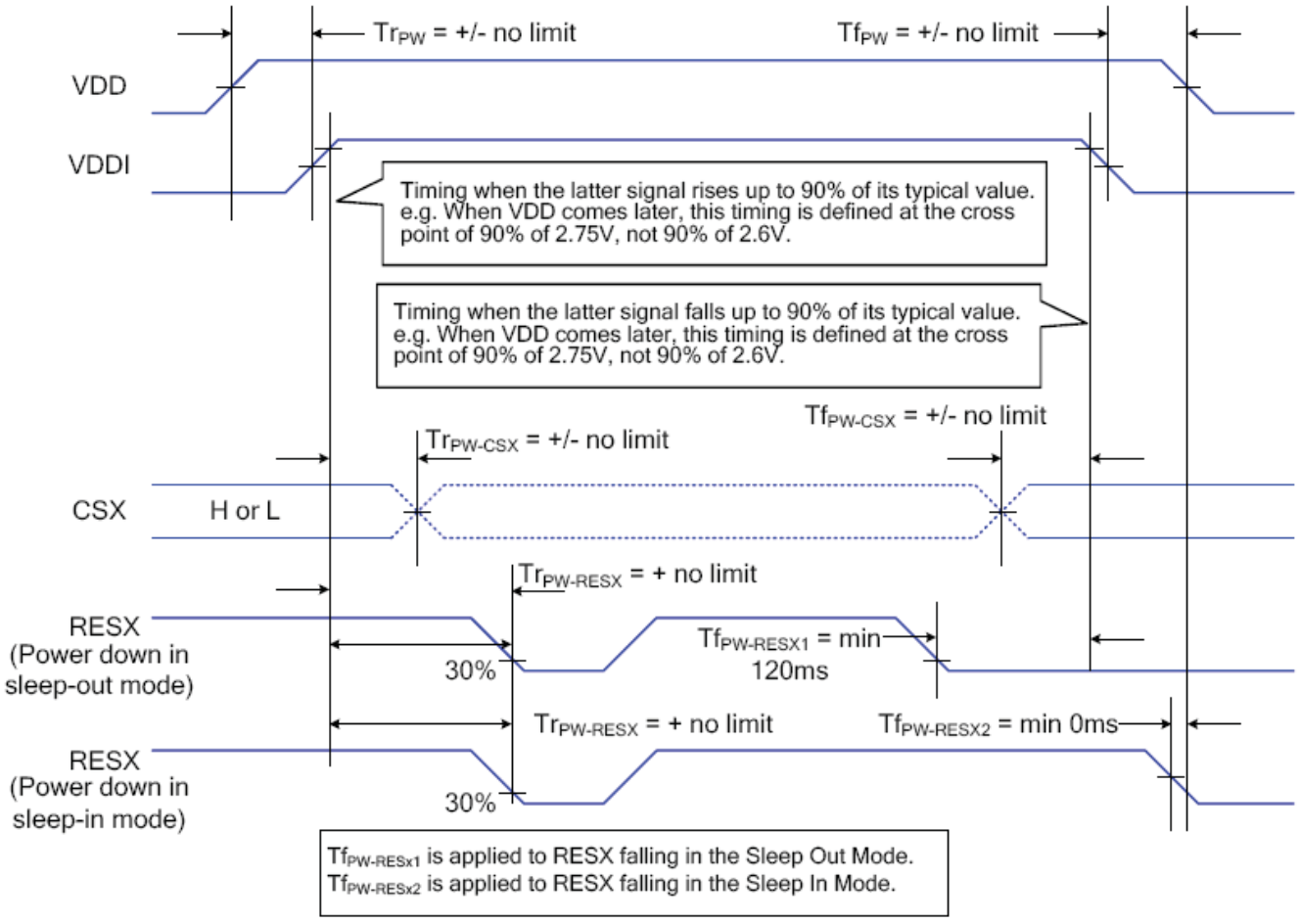
VDDI and VDDA can be applied or powered down in any order. During the Power Off sequence, if the LCD is in the Sleep Out mode, VDDA and VDDI must be powered down with minimum 120msec. If the LCD is in the Sleep In mode, VDDA and VDDI can be powered down with minimum 0msec after the RESX is released.

CSX can be applied at any timing or can be permanently grounded. RESX has high priority over CSX.

Notes:

1. There will be no damage to the ST7701S if the power sequences are not met.
2. There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.
3. There will be no abnormal visible effects on the display between the end of Power On Sequence and before receiving the Sleep Out command, and also between receiving the Sleep In command and the Power Off Sequence.
4. If the RESX line is not steadily held by the host during the Power On Sequence as defined in Sections 9.1 and 9.2, then it will be necessary to apply the Hardware Reset (RESX) after the completion of the Host Power On Sequence to ensure correct operations. Otherwise, all the functions are not guaranteed.

The power on/off sequence is illustrated below



The uncontrolled power-off means a situation which removed a battery without the controlled power off sequence. It will neither damage the module or the host interface.

If uncontrolled power-off happened, the display will go blank and there will not any visible effect on the display (blank display) and remains blank until "Power On Sequence" powers it up.

10. RELIABILITY TEST CONDITIONS

<table>
<tr><th>No.</th><th>Test item</th><th colspan="2">Test condition</th><th>Inspection after test</th></tr>
<tr><td>11.1</td><td>High temperature storage test</td><td colspan="2">+80°C/240 hours</td><td rowspan="11">Inspection after 2~4hours storage at room temperature, the sample shall be free from defects :
1.Current changing value before test and after test is 50% larger;
2. Function defect : Non-display,abnormal-display,missing lines, Short lines,ITO corrosion;
3.Visual defect : Air bubble in the LCD,Seal leak,Glass crack.</td></tr>
<tr><td>11.2</td><td>Low temperature storage test</td><td colspan="2">-30°C/240 hours</td></tr>
<tr><td>11.3</td><td>High temperature operating test</td><td colspan="2">+70°C/120 hours</td></tr>
<tr><td>11.4</td><td>Low temperature operating test</td><td colspan="2">-20°C/120 hours</td></tr>
<tr><td>11.5</td><td>Temperature cycle storage test</td><td colspan="2">-30°C ~ 25°C ~ +80°C/10cycles
(30min.) (10min.) (30min.)</td></tr>
<tr><td>11.6</td><td>High temperature high humidity test</td><td colspan="2">+50°C*90% RH/120 hours</td></tr>
<tr><td>11.7</td><td>Vibration test</td><td colspan="2">Frequency : 250 r/min
Amplitude : 1 inch
Time: 45min</td></tr>
<tr><td rowspan="5">11.8</td><td rowspan="5">Drop test</td><td colspan="2">Drop direction:
1 corner/3 edges/6 sides 10 times</td></tr>
<tr><td>Packing weight(kg)</td><td>Drop height(cm)</td></tr>
<tr><td>〈11</td><td>80±1.6</td></tr>
<tr><td>11≦G〈21</td><td>60±1.2</td></tr>
<tr><td>21≦G〈31</td><td>50±1.0</td></tr>
<tr><td>11.9</td><td>ESD test</td><td colspan="2">Air discharge: ±8KV, 10times
Contact discharge: ±4KV, 10times</td></tr>
</table>

Remark :
1.The test samples should be applied to only one test item.
2.Sample size for each test item is 3~5pcs.
3.For High temperature high humidity test, Pure water(Resistance>10MΩ) should be used.
4.In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judged as a good part.
5.B/L evaluation should be excepted from reliability test with humidity and temperature: Some defects such as black spot/blemish can happen by natural chemical reaction with humidity and Fluorescence B/L has.
6.Failure judgment criterion: Basic specification, Electrical characteristic, Mechanical characteristic, Optical characteristic.

11.INSPECTION CRITERION

Refer to 《Inspection Criterion for TFT Products》 V2.3，DOCUMENT NO.:GTK（WI）-00-QA-007

12. HANDLING PRECAUTIONS

12.1 Mounting method

The LCD module consists of two thin glass plates with polarizes which easily be damaged. And since the module in so constructed as to be fixed by utilizing fitting holes in the printed circuit board.
Extreme care should be needed when handling the LCD modules.

12.2 Caution of LCD handling and cleaning

When cleaning the display surface, Use soft cloth with solvent
[recommended below] and wipe lightly :
●.Isopropyl alcohol
●.Ethyl alcohol
Do not wipe the display surface with dry or hard materials that will damage the polarizer surface.
Do not use the following solvent :
●.Water
●.Aromatics
Do not wipe ITO pad area with the dry or hard materials that will damage the ITO patterns
Do not use the following solvent on the pad or prevent it from being contaminated :
●.Soldering flux
●.Chlorine (Cl) , Sulfur (S)
If goods were sent without being silicon coated on the pad, ITO patterns could be damaged due to the corrosion as time goes on.
If ITO corrosion happen by miss-handling or using some materials such as Chlorine (Cl), Sulfur (S) from customer, Responsibility is on customer.

12.3 Caution against static charge

The LCD module use C-MOS LSI drivers, so we recommended that you :
Connect any unused input terminal to Vdd or Vss, do not input any signals before power is turned on, and ground your body, work/assembly areas, assembly equipment to protect against static electricity.

12.4 Packing

Module employ LCD elements and must be treated as such.
●.Avoid intense shock and falls from a height.
●.To prevent modules from degradation, do not operate or store them exposed direct to sunshine or high temperature/humidity.

12.5 Caution for operation

●.It is an indispensable condition to drive LCD’s within the specified voltage limit since the higher voltage then the limit cause the shorter LCD life.
●.An electrochemical reaction due to direct current causes LCD’s undesirable deterioration, so that the use of direct current drive should be avoided.
●.Response time will be extremely delayed at lower temperature then the operating temperature range and on the other hand at higher temperature LCD’s how dark color in them. However those phenomena do not mean malfunction or out of order with LCD’s, which will come back in the specified operation temperature.
●.If the display area is pushed hard during operation, some font will be abnormally displayed but it resumes normal condition after turning off once.
●.A slight dew depositing on terminals is a cause for electro-chemical reaction resulting in terminal open circuit.
●.Usage under the maximum operating temperature, 50%Rh or less is required.
●.When fixed patterns are displayed for a long time,remnant image is likely to occur.

12.6 Storage

In the case of storing for a long period of time for instance, for years for the purpose or replacement use, the following ways are recommended.
●.Storing in an ambient temperature 10°C to 30°C, and in a relative humidity of 45% to 75%. Don’t expose to sunlight or fluorescent light.
●.Storing in a polyethylene bag with the opening sealed so as not to enter fresh air outside in it . And with no desiccant.
●.Placing in a dark place where neither exposure to direct sunlight nor light’s keeping the storage temperature range.

●.Storing with no touch on polarizer surface by the anything else.
It is recommended to store them as they have been contained in the inner container at the time of delivery from us.

12.7 Safety

●.It is recommendable to crash damaged or unnecessary LCD's into pieces and wash off liquid crystal by either of solvents such as acetone and ethanol, which should be burned up later.
●.When any liquid leaked out of a damaged glass cell comes in contact with your hands, please wash it off well with soap and water.

13. PRECAUTION FOR USE

13.1 A limit sample should be provided by the both parties on an occasion when the both parties agreed its necessity. Judgment by a limit sample shall take effect after the limit sample has been established and confirmed by the both parties.
13.2 On the following occasions, the handing of problem should be decided through discussion and agreement between responsible of the both parties.
●.When a question is arisen in this specification.
●.When a new problem is arisen which is not specified in this specifications.
●.When an inspection specifications change or operating condition change in customer is reported to GTK, and some problem is arisen in this specification due to the change.
●.When a new problem is arisen at the customer's operating set for sample evaluation in the customer site.

14. PACKING SPECIFICATION

Please consult our technical department for detail information.

15. INITIALIZATION CODE

```
HW_Reset();
Delay(120);

WriteComm (0xFF);
WriteData (0x77);
WriteData (0x01);
WriteData (0x00);
WriteData (0x00);
WriteData (0x13);
WriteComm (0xEF);
WriteData (0x08);
WriteComm (0xFF);
WriteData (0x77);
WriteData (0x01);
WriteData (0x00);
WriteData (0x00);
WriteData (0x10);
WriteComm (0xC0);
WriteData (0x77);
WriteData (0x00);
WriteComm (0xC1);
WriteData (0x0C);
WriteData (0x0C);
WriteComm (0xC2);
WriteData (0x27);
WriteData (0x0A);
WriteComm (0xCC);
WriteData (0x10);
WriteComm (0xB0);
WriteData (0x00);
WriteData (0x0C);
WriteData (0x19);
WriteData (0x0B);
WriteData (0x0F);
WriteData (0x06);
WriteData (0x05);
```

```
WriteData (0x08);
WriteData (0x08);
WriteData (0x1F);
WriteData (0x04);
WriteData (0x11);
WriteData (0x0F);
WriteData (0x26);
WriteData (0x2F);
WriteData (0x1D);
WriteComm (0xB1);
WriteData (0x00);
WriteData (0x17);
WriteData (0x19);
WriteData (0x0F);
WriteData (0x12);
WriteData (0x05);
WriteData (0x05);
WriteData (0x08);
WriteData (0x07);
WriteData (0x1F);
WriteData (0x03);
WriteData (0x10);
WriteData (0x10);
WriteData (0x27);
WriteData (0x2F);
WriteData (0x1D);
WriteComm (0xFF);
WriteData (0x77);
WriteData (0x01);
WriteData (0x00);
WriteData (0x00);
WriteData (0x11);
WriteComm (0xB0);
WriteData (0x25);
WriteComm (0xB1);
WriteData (0x76);
WriteComm (0xB2);
WriteData (0x81);
WriteComm (0xB3);
WriteData (0x80);
WriteComm (0xB5);
WriteData (0x4E);
WriteComm (0xB7);
WriteData (0x85);
WriteComm (0xB8);
WriteData (0x20);
WriteComm (0xC1);
WriteData (0x78);
WriteComm (0xC2);
WriteData (0x78);
WriteComm (0xD0);
WriteData (0x88);
WriteComm (0xE0);
WriteData (0x00);
WriteData (0x00);
WriteData (0x02);
WriteComm (0xE1);
WriteData (0x02);
WriteData (0x8C);
WriteData (0x04);
```

```
WriteData (0x8C);
WriteData (0x01);
WriteData (0x8C);
WriteData (0x03);
WriteData (0x8C);
WriteData (0x00);
WriteData (0x44);
WriteData (0x44);
WriteComm (0xE2);
WriteData (0x00);
WriteData (0x00);
WriteData (0x00);
WriteData (0x00);
WriteData (0x00);
WriteData (0x00);
WriteData (0x00);
WriteData (0x00);
WriteData (0x00);
WriteData (0x00);
WriteData (0x00);
WriteData (0x00);
WriteComm (0xE3);
WriteData (0x00);
WriteData (0x00);
WriteData (0x33);
WriteData (0x33);
WriteComm (0xE4);
WriteData (0x44);
WriteData (0x44);
WriteComm (0xE5);
WriteData (0x09);
WriteData (0xD2);
WriteData (0x35);
WriteData (0x8C);
WriteData (0x0B);
WriteData (0xD4);
WriteData (0x35);
WriteData (0x8C);
WriteData (0x05);
WriteData (0xCE);
WriteData (0x35);
WriteData (0x8C);
WriteData (0x07);
WriteData (0xD0);
WriteData (0x35);
WriteData (0x8C);
WriteComm (0xE6);
WriteData (0x00);
WriteData (0x00);
WriteData (0x33);
WriteData (0x33);
WriteComm (0xE7);
WriteData (0x44);
WriteData (0x44);
WriteComm (0xE8);
WriteData (0x08);
WriteData (0xD1);
WriteData (0x35);
WriteData (0x8C);
WriteData (0x0A);
```

```
WriteData (0xD3);
WriteData (0x35);
WriteData (0x8C);
WriteData (0x04);
WriteData (0xCD);
WriteData (0x35);
WriteData (0x8C);
WriteData (0x06);
WriteData (0xCF);
WriteData (0x35);
WriteData (0x8C);
WriteComm (0xEB);
WriteData (0x00);
WriteData (0x01);
WriteData (0xE4);
WriteData (0xE4);
WriteData (0x44);
WriteData (0x00);
WriteComm (0xED);
WriteData (0x77);
WriteData (0x66);
WriteData (0x55);
WriteData (0x44);
WriteData (0xCA);
WriteData (0xF1);
WriteData (0x03);
WriteData (0xBF);
WriteData (0xFB);
WriteData (0x30);
WriteData (0x1F);
WriteData (0xAC);
WriteData (0x44);
WriteData (0x55);
WriteData (0x66);
WriteData (0x77);
WriteComm (0xEF);
WriteData (0x10);
WriteData (0x0D);
WriteData (0x04);
WriteData (0x08);
WriteData (0x3F);
WriteData (0x1F);
WriteComm (0xFF);
WriteData (0x77);
WriteData (0x01);
WriteData (0x00);
WriteData (0x00);
WriteData (0x00);
WriteComm (0x11);
Delay_ms(120);
WriteComm (0x29);
WriteComm (0x36);
WriteData (0x00);
```

16. HSF COMPLIANCE

●.This products complies with ROHS 2011/65/EU and 2015/863/EU、REACH 1907/2006/EC requirements, and the packaging complies with 94-62-EC.